



# PSMN4R2-60PL

N-channel 60 V, 3.9 mΩ logic level MOSFET in SOT78

5 February 2013

Product data sheet

## 1. General description

Logic level N-channel MOSFET in SOT78 using TrenchMOS technology. Product design and manufacture has been optimized for use in battery operated power tools.

## 2. Features and benefits

- High efficiency due to low switching & conduction losses
- Robust construction for demanding applications
- Logic level gate

## 3. Applications

- Battery-powered tools
- Load switching
- Motor control
- Uninterruptible power supplies

## 4. Quick reference data

Table 1. Quick reference data

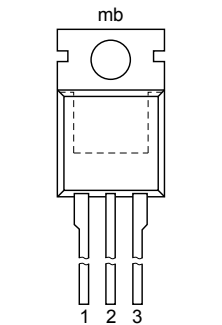
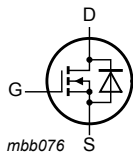
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	60	V	
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ <a href="#">Fig. 1</a>	[1]	-	130	A	
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ <a href="#">Fig. 2</a>	-	-	263	W	
<b>Static characteristics</b>							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C};$ <a href="#">Fig. 11</a>	-	3.17	3.9	mΩ	
<b>Dynamic characteristics</b>							
$Q_{G(tot)}$	total gate charge	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; V_{DS} = 48\text{ V};$ <a href="#">Fig. 13; Fig. 14</a>	-	151	-	nC	
$Q_{GD}$	gate-drain charge		-	27	-	nC	
<b>Avalanche ruggedness</b>							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 130\text{ A}; V_{sup} \leq 60\text{ V}; R_{GS} = 50\text{ Ω};$ $V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C};$ unclamped; <a href="#">Fig. 3</a>	-	-	283	mJ	

[1] Continuous current is limited by package.



## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>TO-220AB (SOT78)</p>	 <p>mbb076</p>
2	D	drain		
3	S	source		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN4R2-60PL	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN4R2-60PL	PSMN4R2-60PL

## 8. Limiting values

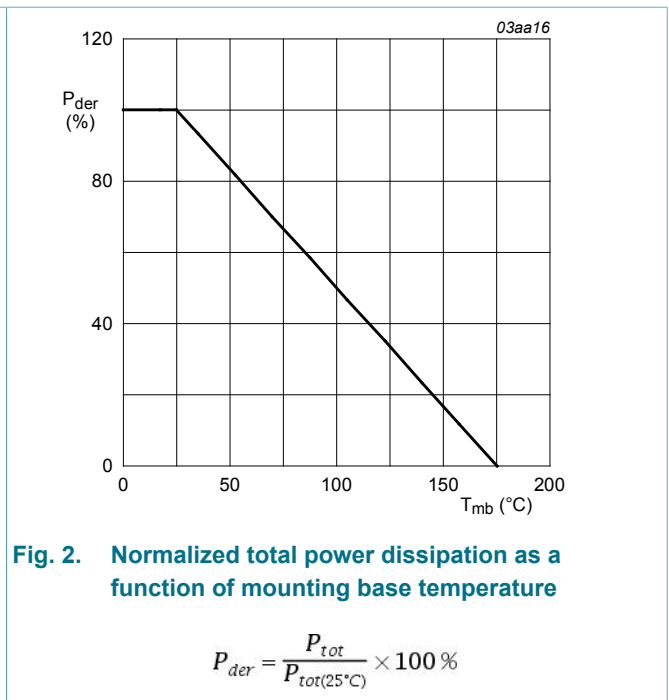
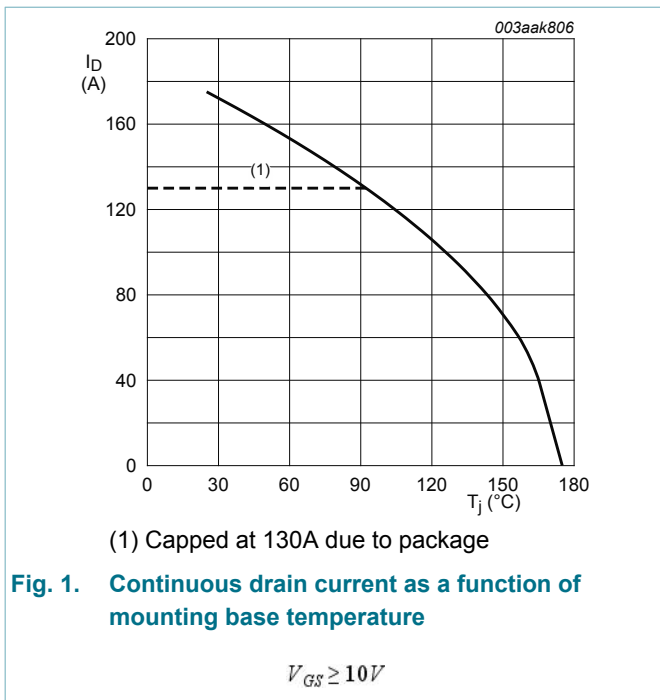
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	60	V	
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	60	V	
$V_{GS}$	gate-source voltage		-20	20	V	
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; Fig. 1	[1]	-	130	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; Fig. 1		-	124	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; Fig. 4	-	701	A	

Symbol	Parameter	Conditions		Min	Max	Unit
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>		-	263	W
T <sub>stg</sub>	storage temperature			-55	175	°C
T <sub>j</sub>	junction temperature			-55	175	°C
T <sub>slid(M)</sub>	peak soldering temperature			-	260	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	<a href="#">[1]</a>	-	130	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	701	A
<b>Avalanche ruggedness</b>						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 130 A; V <sub>sup</sub> ≤ 60 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped; <a href="#">Fig. 3</a>		-	283	mJ

[1] Continuous current is limited by package.



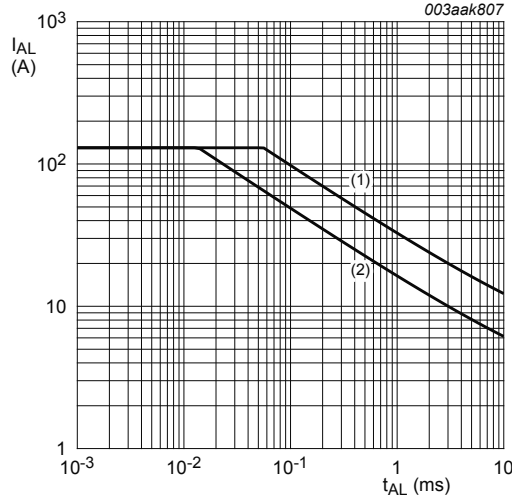


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time

(1)  $T_{j (init)} = 25^{\circ}C$ ; (2)  $T_{j (init)} = 100^{\circ}C$

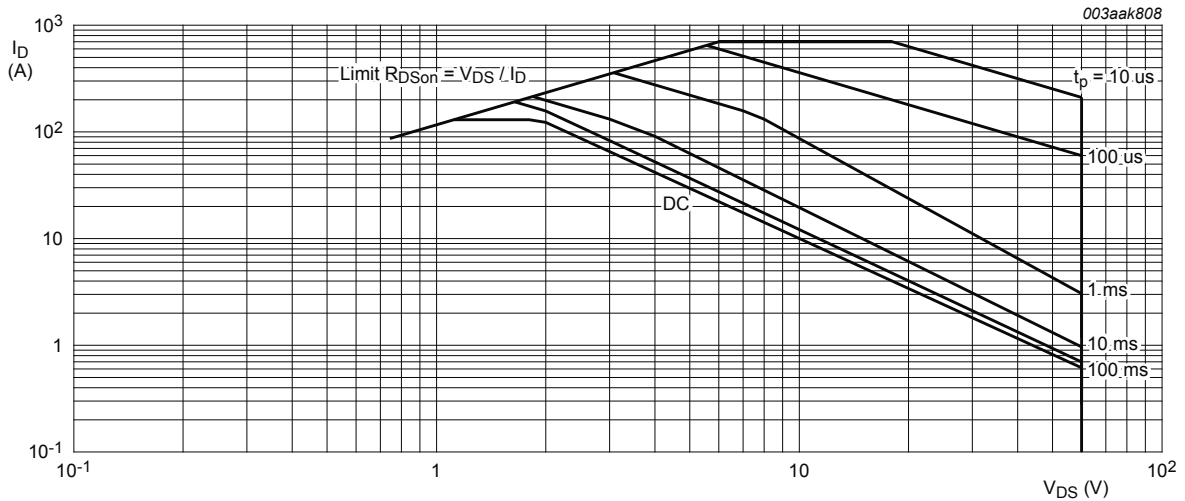


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is a single pulse

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.49	0.57	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air	-	60	-	K/W

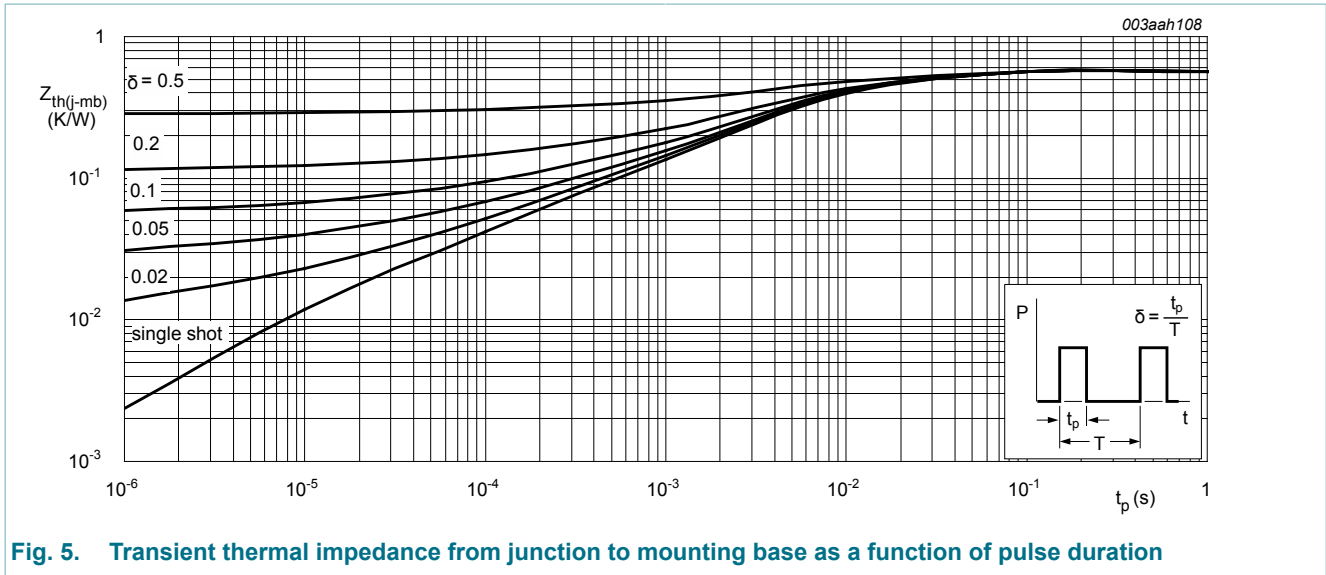


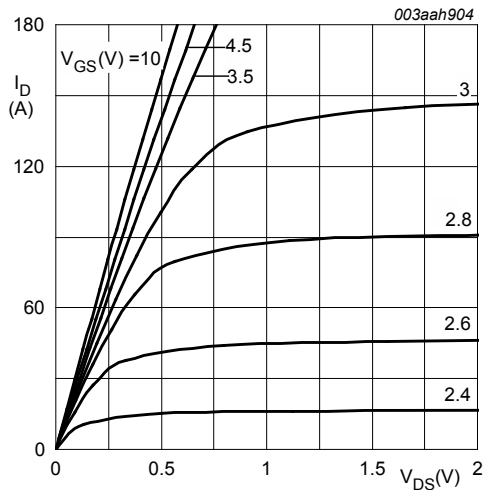
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	60	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	54	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 9; Fig. 10</a>	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ <a href="#">Fig. 9</a>	-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 9</a>	0.5	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.06	1	$\mu A$
		$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	3.6	4.3	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	3.17	3.9	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 12; Fig. 11</a>	-	-	8.6	mΩ
$R_G$	gate resistance	$f = 1 \text{ MHz}$	0.35	0.7	1.4	Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 48 V; V <sub>GS</sub> = 10 V; Fig. 13; Fig. 14	-	151	-	nC
		I <sub>D</sub> = 25 A; V <sub>DS</sub> = 48 V; V <sub>GS</sub> = 5 V; Fig. 13; Fig. 14	-	72	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 48 V; V <sub>GS</sub> = 10 V; Fig. 13; Fig. 14	-	20	-	nC
Q <sub>GD</sub>	gate-drain charge		-	27	-	nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz;	-	8533	-	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; Fig. 15	-	703	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	357	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 45 V; R <sub>L</sub> = 1.8 Ω; V <sub>GS</sub> = 5 V; R <sub>G(ext)</sub> = 5 Ω	-	47	-	ns
t <sub>r</sub>	rise time		-	97	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	84	-	ns
t <sub>f</sub>	fall time		-	73	-	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; Fig. 16	-	0.8	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V;	-	40	-	ns
Q <sub>r</sub>	recovered charge	V <sub>DS</sub> = 25 V	-	59	-	nC



T<sub>j</sub> = 25 °C; t<sub>p</sub> = 300 μs

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

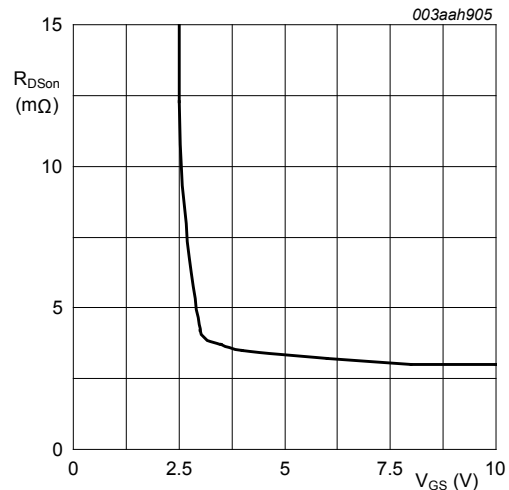
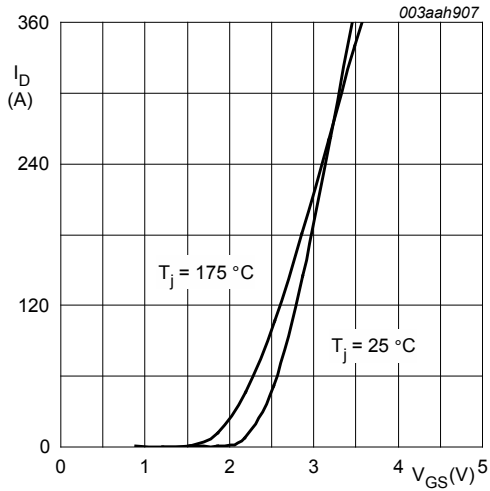


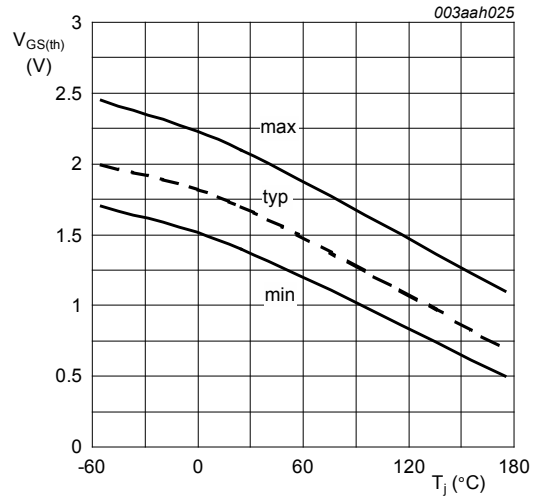
Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

T<sub>j</sub> = 25 °C; I<sub>D</sub> = 25 A



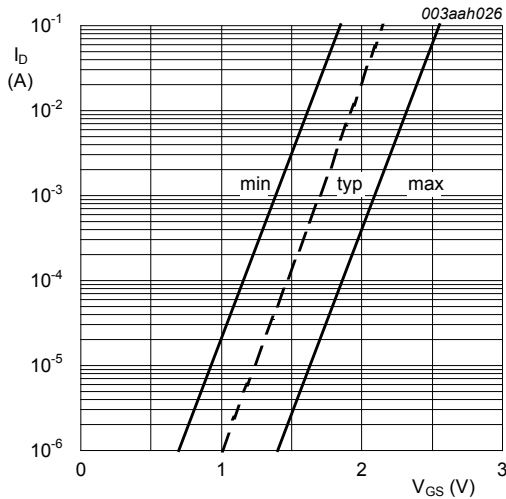
**Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values**

$V_{DS} = 10V$



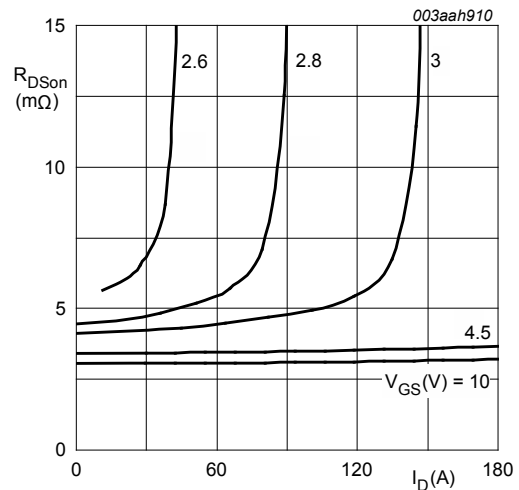
**Fig. 9. Gate-source threshold voltage as a function of junction temperature**

$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$



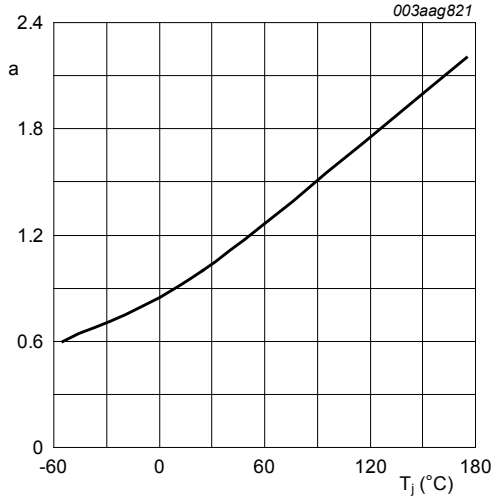
**Fig. 10. Sub-threshold drain current as a function of gate-source voltage**

$T_j = 25^\circ\text{C}; V_{DS} = 5V$



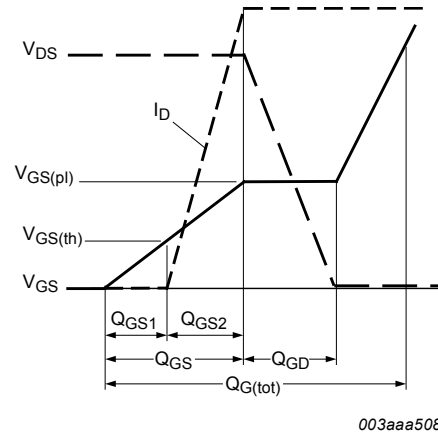
$T_j = 25^\circ\text{C}; t_p = 300 \mu\text{s}$

**Fig. 11. Drain-source on-state resistance as a function of drain current; typical values**

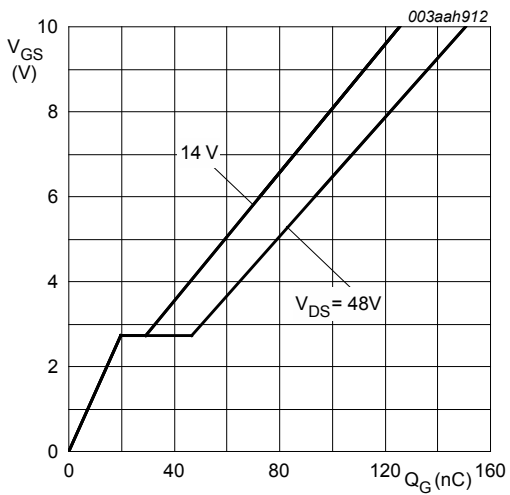


**Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature**

$$a = \frac{R_{DS(on)}}{R_{DS(on)(25\text{ }^\circ\text{C})}}$$

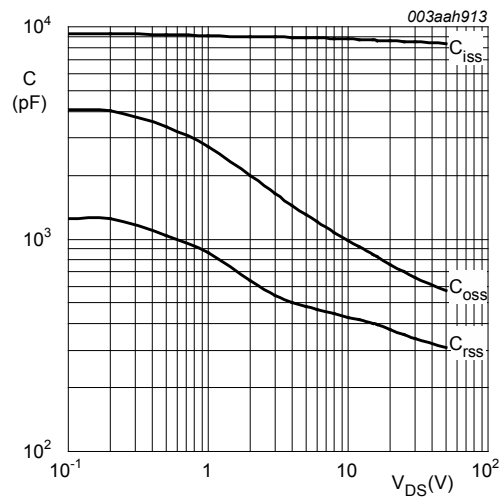


**Fig. 13. Gate charge waveform definitions**



**Fig. 14. Gate-source voltage as a function of gate charge; typical values**

$$T_j = 25^\circ\text{C}; I_D = 25\text{A}$$



**Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

$$V_{GS} = 0\text{V}; f = 1\text{MHz}$$



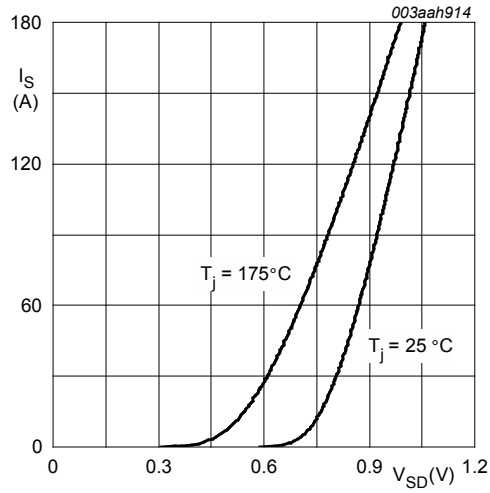


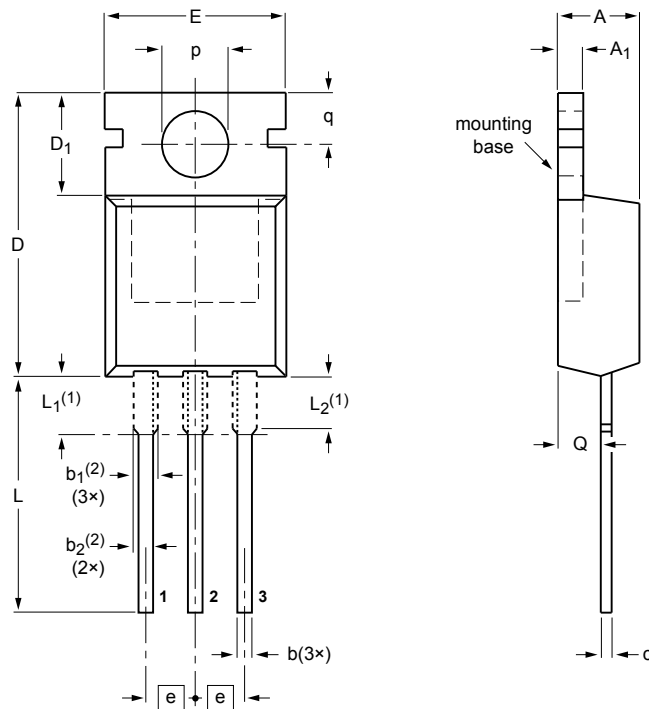
Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

### 11. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	b <sub>1</sub> (2)	b <sub>2</sub> (2)	c	D	D <sub>1</sub>	E	e	L	L <sub>1</sub> (1)	L <sub>2</sub> (1) max.	p	q	Q
mm	4.7 4.1	1.40 1.25	0.9 0.6	1.6 1.0	1.3 1.0	0.7 0.4	16.0 15.2	6.6 5.9	10.3 9.7	2.54	15.0 12.8	3.30 2.79	3.0	3.8 3.5	3.0 2.7	2.6 2.2

**Notes**

- 1. Lead shoulder designs may vary.
- 2. Dimension includes excess dambar.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT78		3-lead TO-220AB	SC-46		08-04-23 08-06-13

Fig. 17. Package outline TO-220AB (SOT78)

## 12. Legal information

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## 13. Contents

1	General description .....	1
2	Features and benefits .....	1
3	Applications .....	1
4	Quick reference data .....	1
5	Pinning information .....	2
6	Ordering information .....	2
7	Marking .....	2
8	Limiting values .....	2
9	Thermal characteristics .....	4
10	Characteristics .....	5
11	Package outline .....	10
12	Legal information .....	11
12.1	Data sheet status .....	11
12.2	Definitions .....	11
12.3	Disclaimers .....	11
12.4	Trademarks .....	12

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Date of release: 5 February 2013