



# PSMN1R5-30YLC

N-channel 30 V 1.55mΩ logic level MOSFET in LPAK using NextPower technology

Rev. 2 — 17 May 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level enhancement mode N-channel MOSFET in LPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

### 1.2 Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, and QOSS for high system efficiencies at low and high loads
- Ultra low R<sub>dson</sub> and low parasitic inductance

### 1.3 Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching
- Power OR-ing
- Server power supplies
- Sync rectifier

### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C	-	-	30	V
I <sub>D</sub>	drain current	T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 10 V; see <a href="#">Figure 1</a>	<a href="#">11</a>	-	100	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <a href="#">Figure 2</a>	-	-	179	W
T <sub>j</sub>	junction temperature		-55	-	175	°C

#### Static characteristics

R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 12</a>	-	1.65	2.05	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; see <a href="#">Figure 12</a>	-	1.3	1.55	mΩ



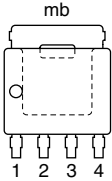
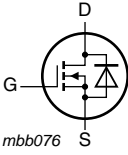
**Table 1. Quick reference data ...continued**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 4.5\text{ V}$ ; $I_D = 25\text{ A}$ ; $V_{DS} = 15\text{ V}$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	8.6	-	nC
$Q_{G(tot)}$	total gate charge	$V_{GS} = 4.5\text{ V}$ ; $I_D = 25\text{ A}$ ; $V_{DS} = 15\text{ V}$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	30	-	nC

[1] Continuous current is limited by package.

## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

**SOT669 (LPAK; Power-SO8)**

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
PSMN1R5-30YLC	LPAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669

## 4. Marking

**Table 4. Marking codes**

Type number	Marking code <sup>[1]</sup>
PSMN1R5-30YLC	1C530L

[1] % = placeholder for manufacturing site code

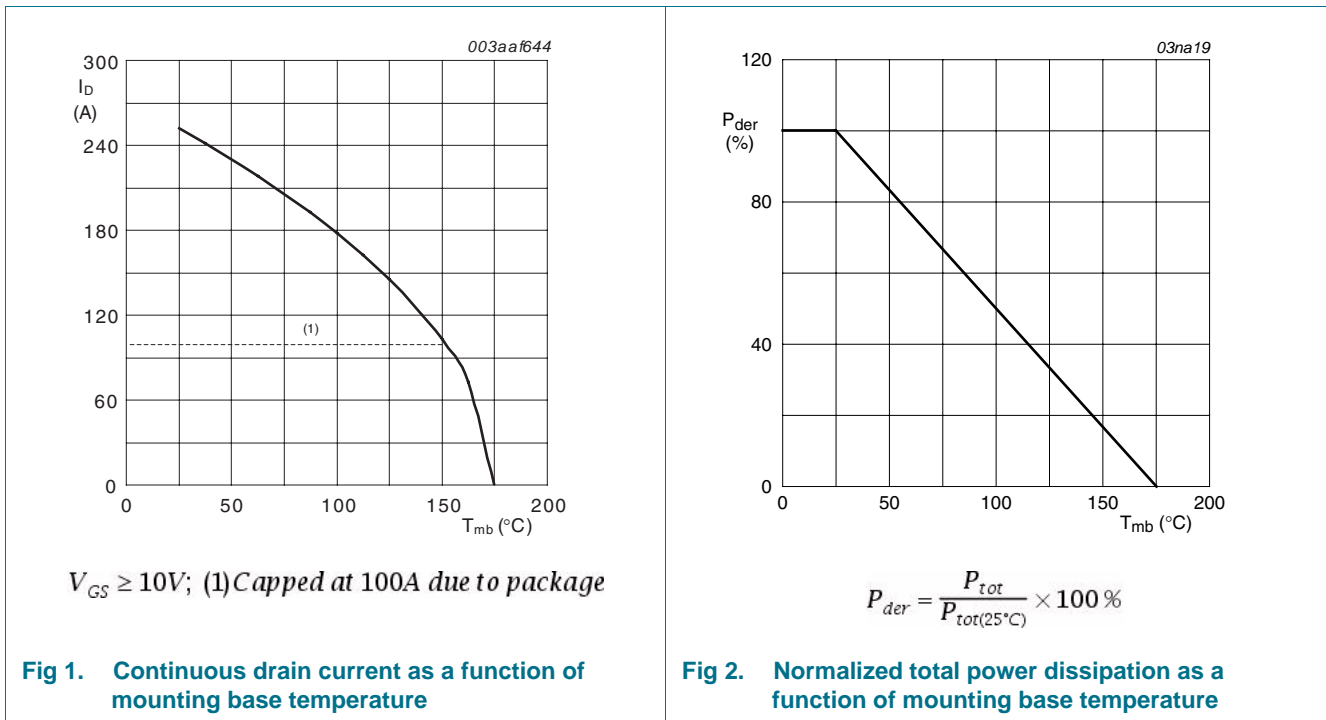
### 5. Limiting values

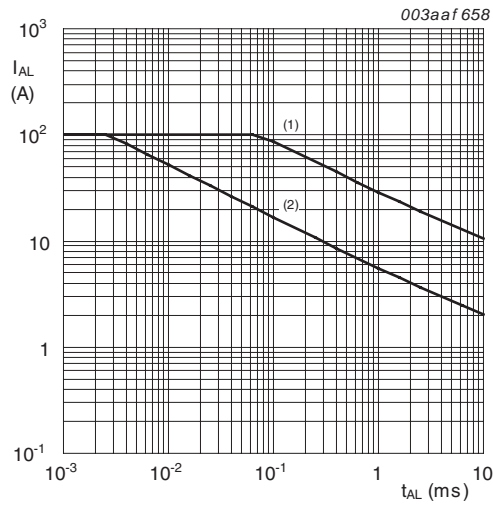
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C	-	30	V
V <sub>DGR</sub>	drain-gate voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C; R <sub>GS</sub> = 20 kΩ	-	30	V
V <sub>GS</sub>	gate-source voltage		-20	20	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; see <a href="#">Figure 1</a>	[1]	100	A
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; see <a href="#">Figure 1</a>	[1]	100	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; see <a href="#">Figure 4</a>	-	1008	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; see <a href="#">Figure 2</a>	-	179	W
T <sub>stg</sub>	storage temperature		-55	175	°C
T <sub>j</sub>	junction temperature		-55	175	°C
T <sub>slid(M)</sub>	peak soldering temperature		-	260	°C
V <sub>ESD</sub>	electrostatic discharge voltage	MM (JEDEC JESD22-A115)	1000	-	V
<b>Source-drain diode</b>					
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	[1]	100	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C	-	1008	A
<b>Avalanche ruggedness</b>					
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; I <sub>D</sub> = 100 A; V <sub>sup</sub> ≤ 30 V; R <sub>GS</sub> = 50 Ω; unclamped; see <a href="#">Figure 3</a>	-	147	mJ

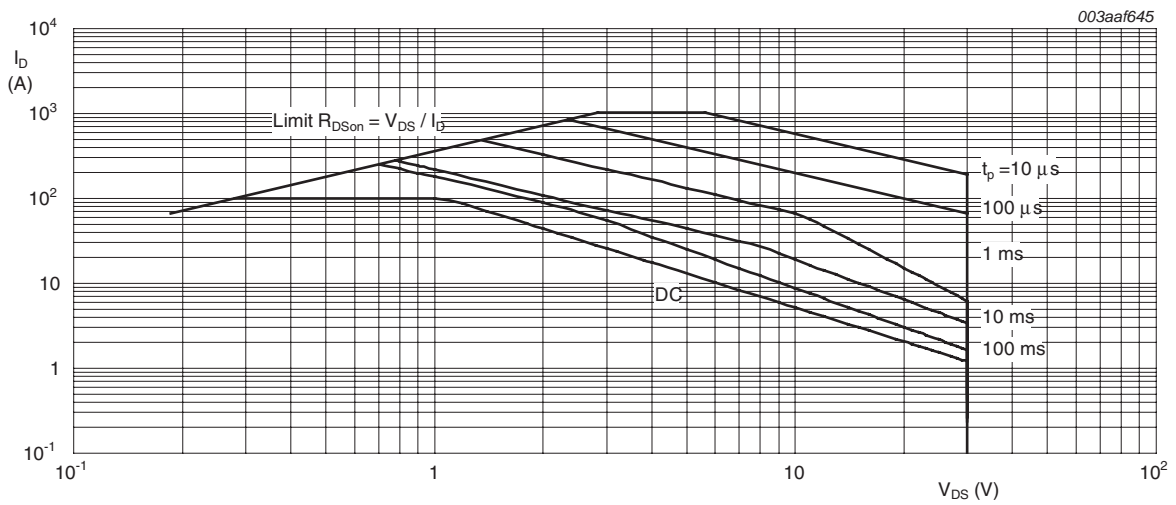
[1] Continuous current is limited by package.





(1)  $T_{j (limit)} = 25^{\circ}C$ ; (2)  $T_{j (limit)} = 100^{\circ}C$

Fig 3. Single pulse avalanche rating; avalanche current as a function of avalanche time



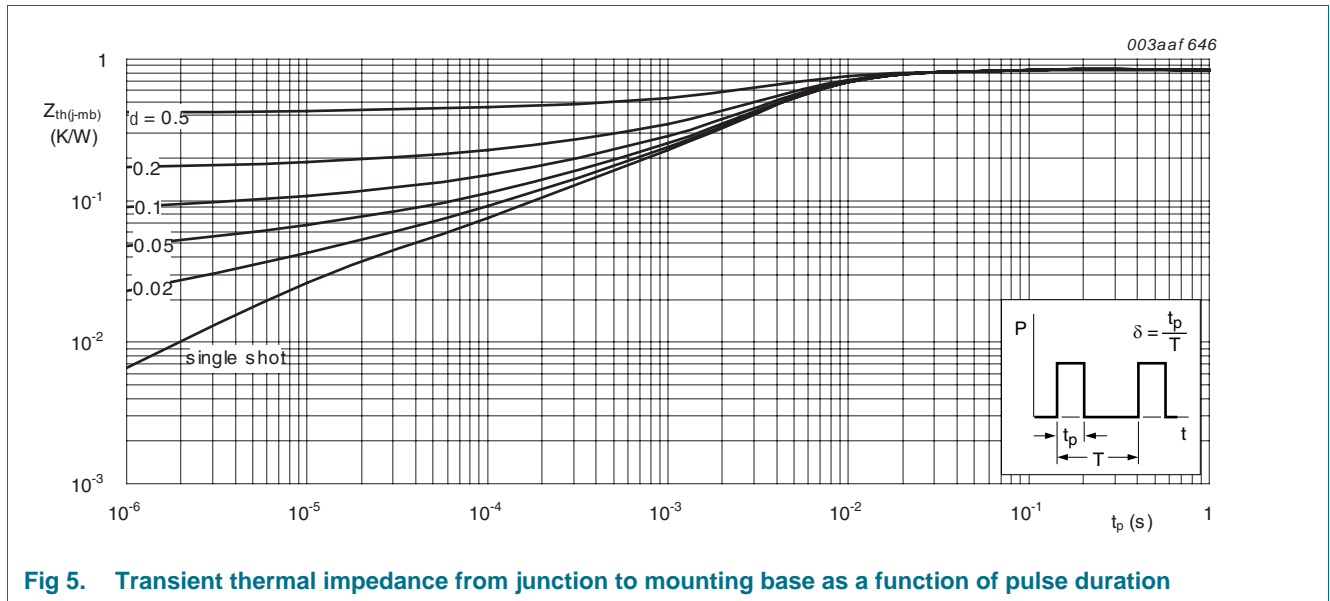
$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is a single pulse

Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## 6. Thermal characteristics

**Table 6. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 5</a>	-	0.71	0.84	K/W



**Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	30	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	1.05	1.51	1.95	V
		$I_D = 10 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ C$	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$	-	-	2.25	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	$\mu A$
		$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 150 \text{ }^\circ C$	-	-	100	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 12</a>	-	1.65	2.05	mΩ
		$V_{GS} = 4.5 V; I_D = 25 A; T_j = 150 \text{ }^\circ C$ ; see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	-	3.4	mΩ
		$V_{GS} = 10 V; I_D = 25 A; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 12</a>	-	1.3	1.55	mΩ
		$V_{GS} = 10 V; I_D = 25 A; T_j = 150 \text{ }^\circ C$ ; see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	-	2.6	mΩ
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	1.05	2.1	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 A; V_{DS} = 15 V; V_{GS} = 10 V$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	65	-	nC
		$I_D = 25 A; V_{DS} = 15 V; V_{GS} = 4.5 V$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	30	-	nC
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$	-	53	-	nC
$Q_{GS}$	gate-source charge	$I_D = 25 A; V_{DS} = 15 V; V_{GS} = 4.5 V$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	9.7	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	6.6	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	3.1	-	nC
$Q_{GD}$	gate-drain charge		-	8.6	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 A; V_{DS} = 15 V$ ; see <a href="#">Figure 14</a> ; see <a href="#">Figure 15</a>	-	2.53	-	V
$C_{iss}$	input capacitance	$V_{DS} = 15 V; V_{GS} = 0 V; f = 1 \text{ MHz}$ ;	-	4044	-	pF
$C_{oss}$	output capacitance	$T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 16</a>	-	860	-	pF
$C_{riss}$	reverse transfer capacitance		-	287	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15 V; R_L = 0.6 \text{ } \Omega; V_{GS} = 4.5 V$ ;	-	33	-	ns
$t_r$	rise time	$R_{G(ext)} = 4.7 \text{ } \Omega$	-	62	-	ns
$t_{d(off)}$	turn-off delay time		-	62	-	ns
$t_f$	fall time		-	38	-	ns

Table 7. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{OSS}$	output charge	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 15\text{ V}$ ; $f = 1\text{ MHz}$ ; $T_j = 25\text{ °C}$	-	23	-	nC
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 17</a>	-	0.8	1.1	V
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ;	-	41	-	ns
$Q_r$	recovered charge	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 15\text{ V}$	-	43	-	nC
$t_a$	reverse recovery rise time	$V_{GS} = 0\text{ V}$ ; $I_S = 25\text{ A}$ ;	-	24	-	ns
$t_b$	reverse recovery fall time	$di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{DS} = 15\text{ V}$ ; see <a href="#">Figure 18</a>	-	17	-	ns

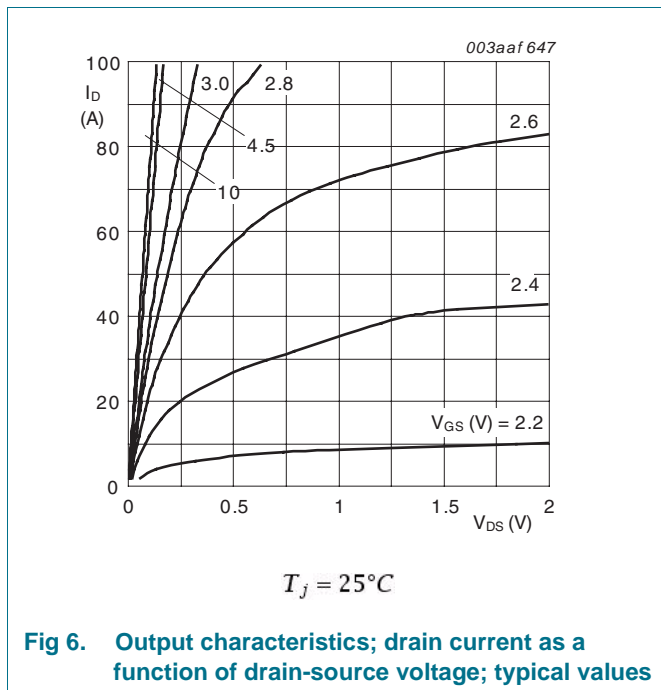


Fig 6. Output characteristics; drain current as a function of drain-source voltage; typical values

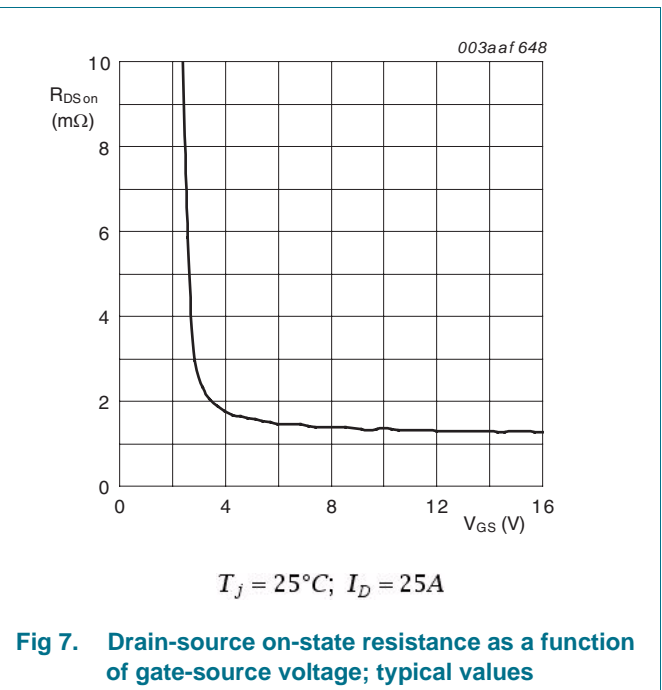
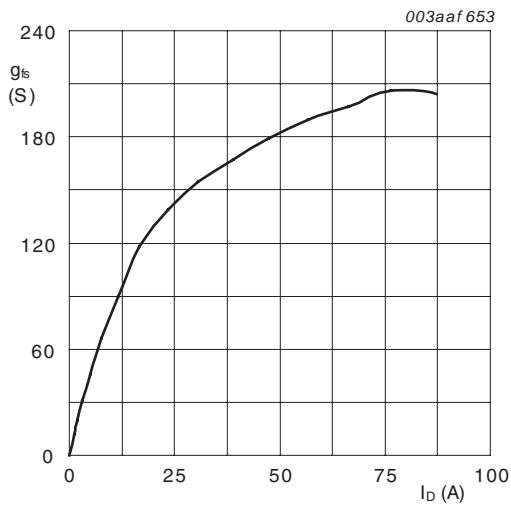
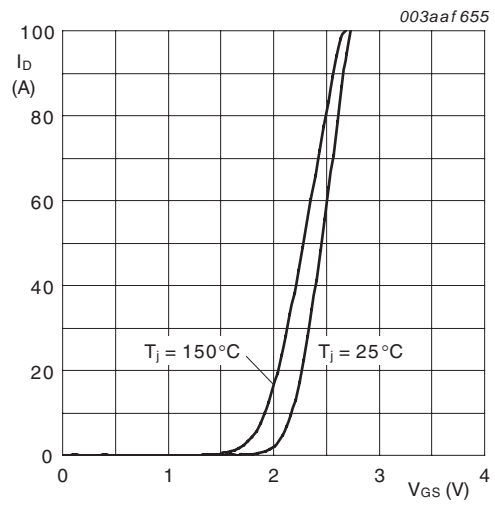


Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



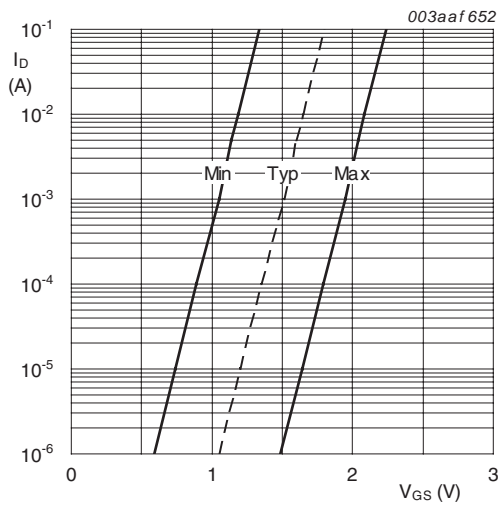
$T_j = 25^\circ\text{C}; V_{DS} = 10\text{V}$

Fig 8. Forward transconductance as a function of drain current; typical values



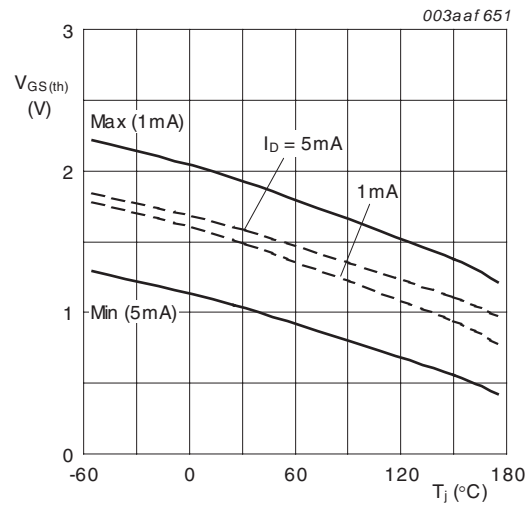
$V_{DS} = 10\text{V}$

Fig 9. Transfer characteristics; drain-source current as a function of gate-source voltage; typical values



$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$V_{DS} = V_{GS}$

Fig 11. Gate-source threshold voltage as a function of junction temperature



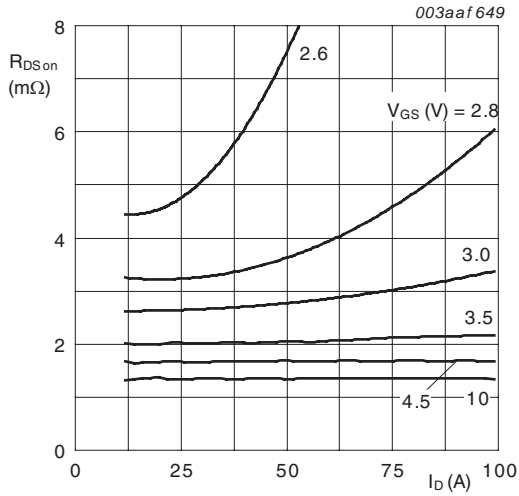
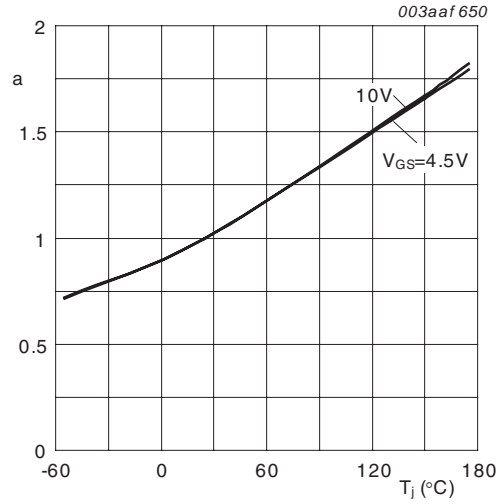


Fig 12. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ C)}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

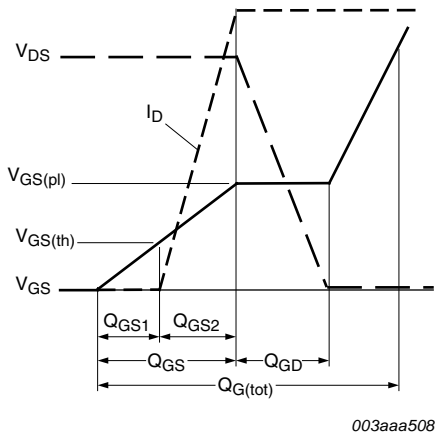
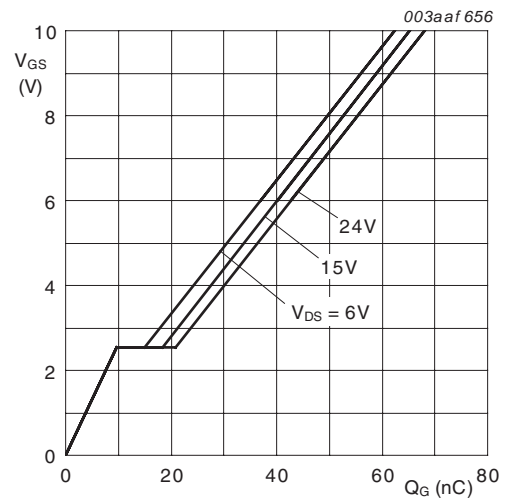
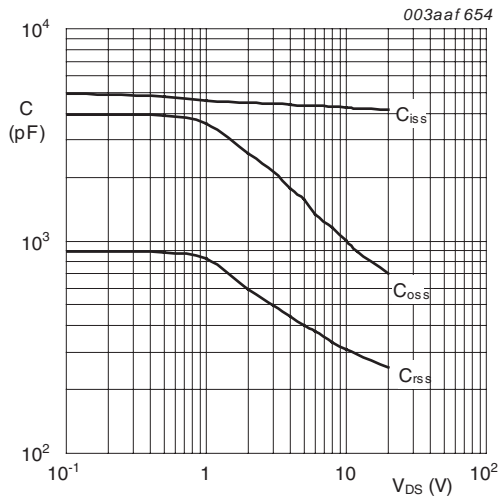


Fig 14. Gate charge waveform definitions



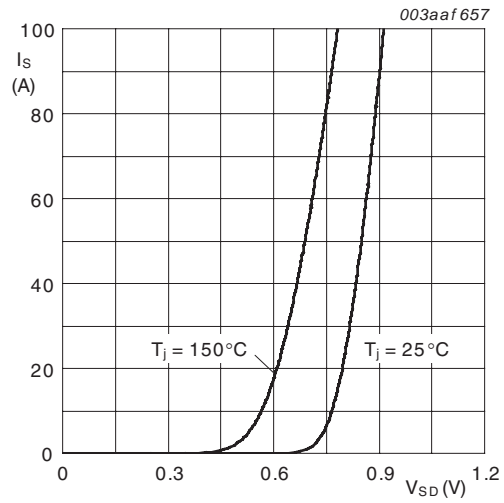
$$T_j = 25^\circ C; I_D = 25A$$

Fig 15. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0V; f = 1MHz$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0V$

Fig 17. Source current as a function of source-drain voltage; typical values

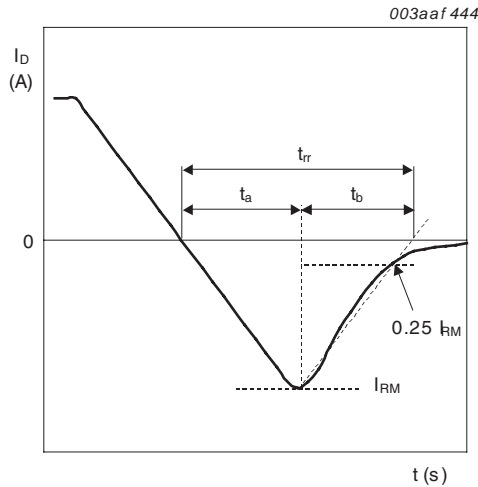


Fig 18. Reverse recovery timing definition

8. Package outline

Plastic single-ended surface-mounted package (LPAK; Power-SO8); 4 leads

SOT669



Fig 19. Package outline SOT669 (LPAK; Power-SO8)

## 9. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN1R5-30YLC v.2	20110517	Product data sheet	-	PSMN1R9-25YLC v.1
Modifications:	• Various changes to content.			
PSMN1R9-25YLC v.1	20110502	Product data sheet	-	-

## 10. Legal information

### 10.1 Data sheet status

Document status <sup>[1]</sup> <sup>[2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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**12. Contents**

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