

PSMN1R3-30YL

N-channel 30 V 1.3 mΩ logic level MOSFET in LPAK

Rev. 02 — 25 June 2009

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel MOSFET in LPAK package qualified to 150 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- Advanced TrenchMOS provides low RDSon and low gate charge
- High efficiency gains in switching power convertors
- Improved mechanical and thermal characteristics
- LPAK provides maximum power density in a Power SO8 package

1.3 Applications

- DC-to-DC converters
- Lithium-ion battery protection
- Load switching
- Motor control
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 150 °C	-	-	30	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; see Figure 1 ;	[1]	-	100	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	-	121	W
T _j	junction temperature		-55	-	150	°C
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 100 A; V _{sup} ≤ 30 V; R _{GS} = 50 Ω; unclamped	-	-	383	mJ
Dynamic characteristics						
Q _{GD}	gate-drain charge	V _{GS} = 4.5 V; I _D = 25 A;	-	9.3	-	nC
Q _{G(tot)}	total gate charge	V _{DS} = 12 V; see Figure 13 ; see Figure 14	-	46.6	-	nC

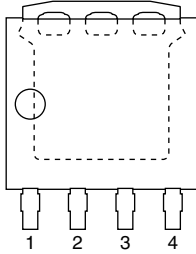
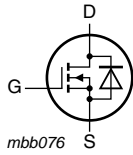
Table 1. Quick reference ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 15\text{ A}; T_j = 100\text{ }^\circ\text{C};$ see Figure 12	-	-	1.8	mΩ
		$V_{GS} = 10\text{ V}; I_D = 15\text{ A}; T_j = 25\text{ }^\circ\text{C};$ see Figure 17	-	1.04	1.3	mΩ

[1] Continuous current is limited by package.

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p style="text-align: center;">SOT1023 (LFAK2)</p>	 <p style="text-align: center;"><i>mbb076</i></p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PSMN1R3-30YL	LFAK2	Plastic single-ende surface-mounted package (LFAK2); 4 leads	SOT1023

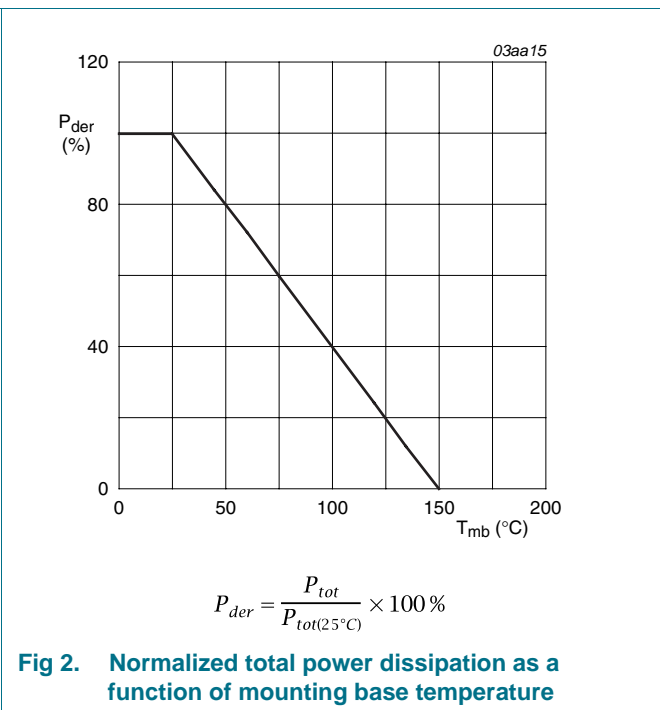
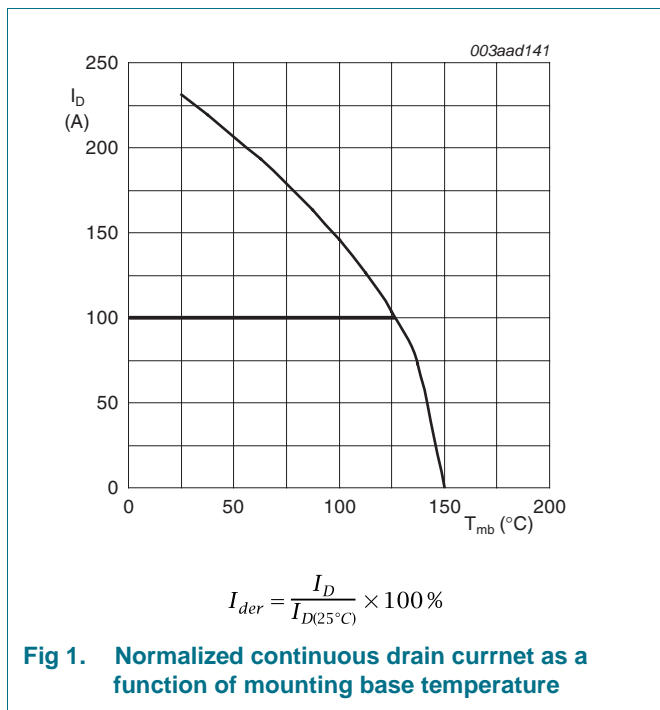
4. Limiting values

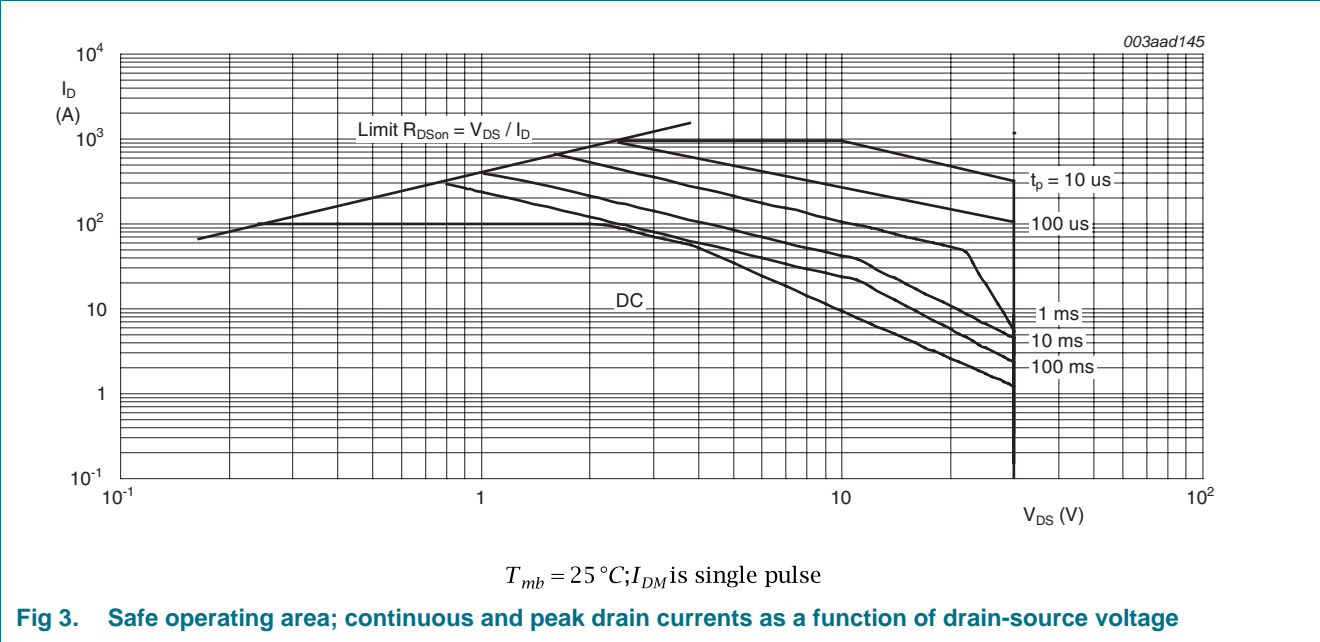
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 150 °C	-	30	V
V _{DGR}	drain-gate voltage	T _j ≥ 25 °C; T _j ≤ 150 °C; R _{GS} = 20 kΩ	-	30	V
V _{GS}	gate-source voltage		-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 100 °C; see Figure 1	[1]	100	A
		V _{GS} = 10 V; T _{mb} = 25 °C; see Figure 1	[1]	100	A
I _{DM}	peak drain current	t _p ≤ 10 μs; pulsed; T _{mb} = 25 °C; see Figure 3	-	923	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; see Figure 2	-	121	W
T _{stg}	storage temperature		-55	150	°C
T _j	junction temperature		-55	150	°C
T _{slid(M)}	peak soldering temperature		-	260	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C;	[1]	100	A
I _{SM}	peak source current	t _p ≤ 10 μs; pulsed; T _{mb} = 25 °C	-	923	A
Avalanche ruggedness					
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 100 A; V _{sup} ≤ 30 V; R _{GS} = 50 Ω; unclamped	-	383	mJ

[1] Continuous current is limited by package.





5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	0.4	1.03	K/W

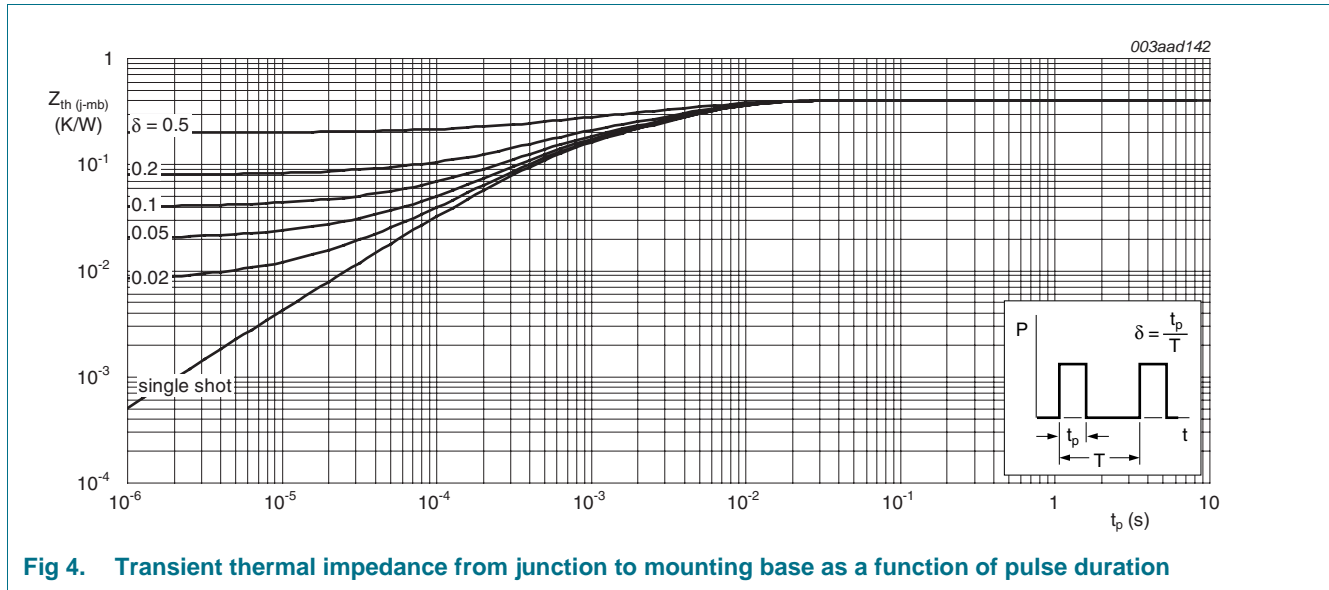


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

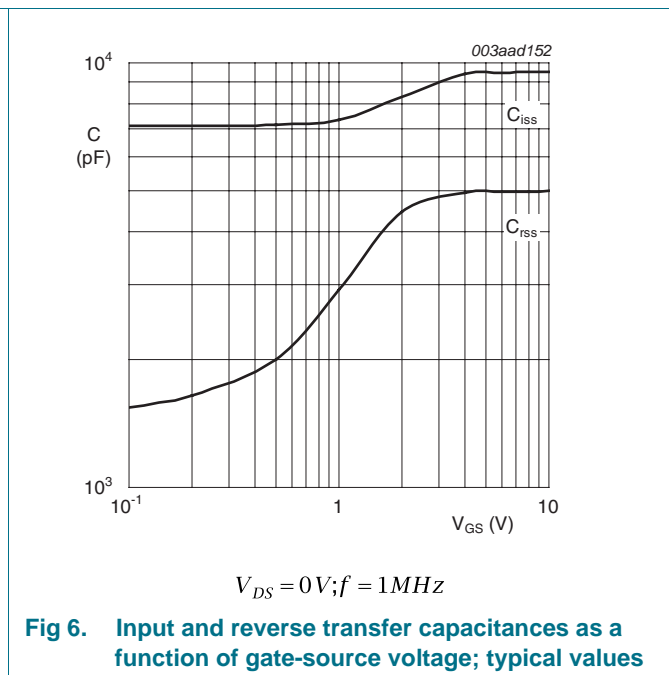
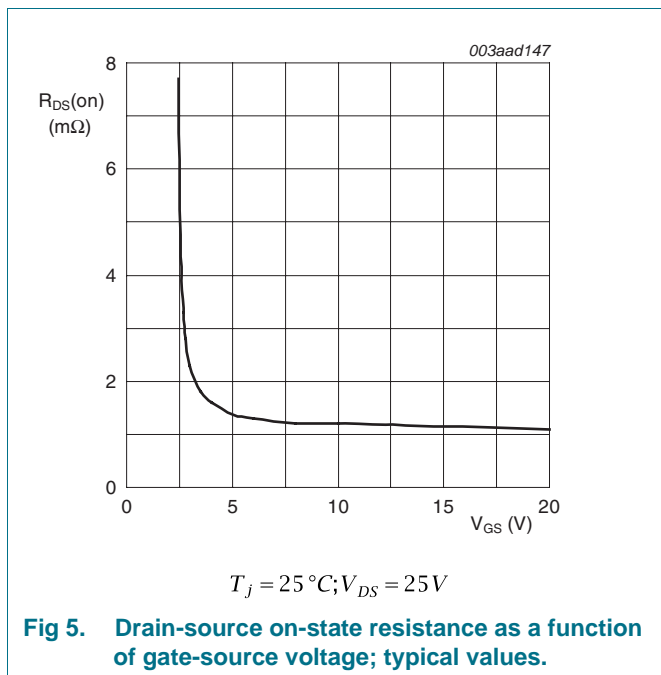
6. Characteristics

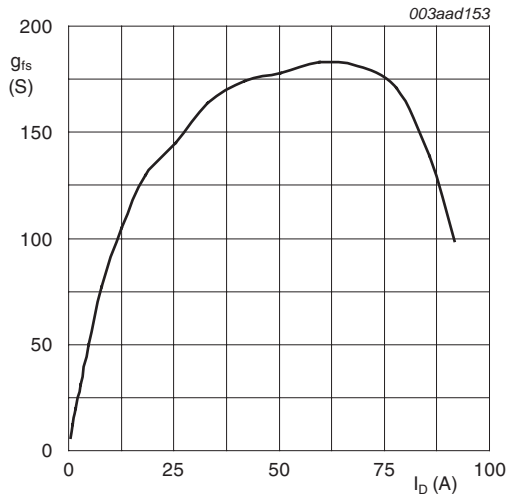
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	30	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 10 ; see Figure 11	1.3	1.7	2.15	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C};$ see Figure 10	0.65	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see Figure 10	-	-	2.45	V
I_{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	1	μA
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 15 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -15 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 17	-	1.43	1.95	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 100 \text{ }^\circ\text{C};$ see Figure 12	-	-	1.8	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ see Figure 12	-	1.9	2.8	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see Figure 17	-	1.04	1.3	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}$	-	0.89	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 10 \text{ V};$ see Figure 13 ; see Figure 14	-	100	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	90	-	nC
		$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$ see Figure 13 ; see Figure 14	-	46.6	-	nC
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$ see Figure 13 ; see Figure 14	-	17.9	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$ see Figure 13	-	11	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	6.9	-	nC
Q_{GD}	gate-drain charge	$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V}; V_{GS} = 4.5 \text{ V};$ see Figure 13 ; see Figure 14	-	9.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$V_{DS} = 12 \text{ V};$ see Figure 13 ; see Figure 14	-	2.53	-	V
C_{iss}	input capacitance	$V_{DS} = 12 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see Figure 15	-	6227	-	pF
C_{oss}	output capacitance		-	1415	-	pF
C_{rss}	reverse transfer capacitance		-	619	-	pF

Table 6. Characteristics ...continued

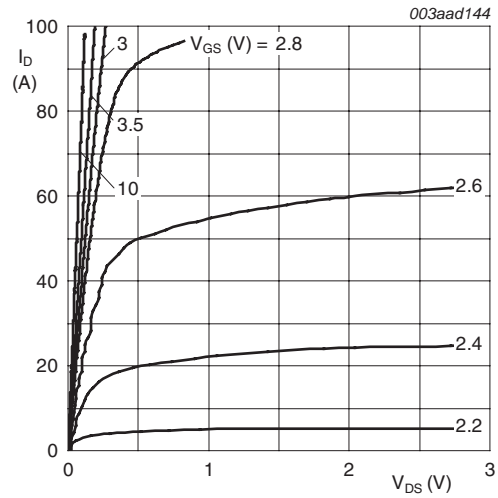
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\text{ V}; R_L = 0.5\ \Omega; V_{GS} = 4.5\text{ V};$	-	64	-	ns
t_r	rise time	$R_{G(ext)} = 5.6\ \Omega$	-	108	-	ns
$t_{d(off)}$	turn-off delay time		-	106	-	ns
t_f	fall time		-	52	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ see Figure 16	-	0.88	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}; di_S/dt = -100\text{ A/s}; V_{GS} = 0\text{ V};$	-	46	-	ns
Q_r	recovered charge	$V_{DS} = 20\text{ V}$	-	53	-	nC





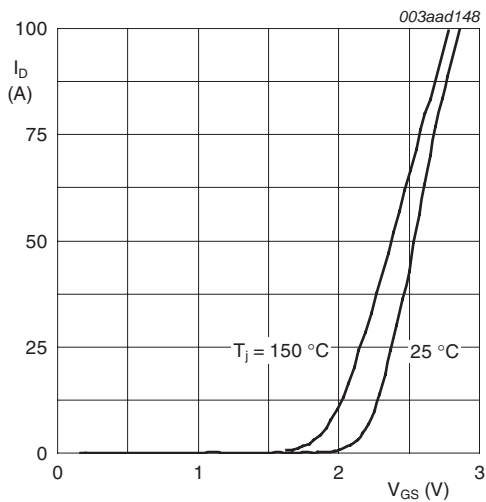
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 25\text{ V}$

Fig 7. Forward transconductance as a function of drain current; typical values



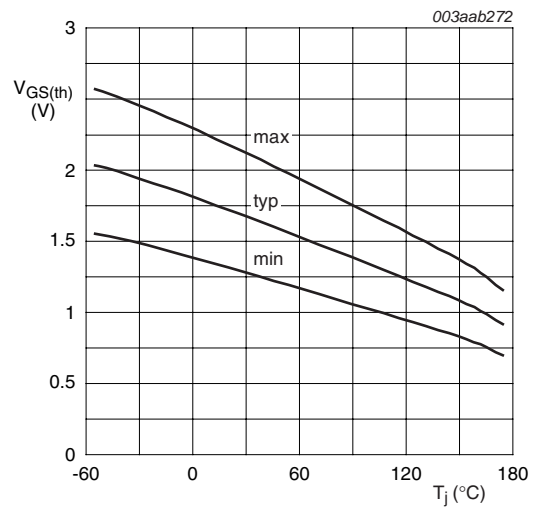
$T_j = 25\text{ }^\circ\text{C}$

Fig 8. Output characteristics: drain current as a function of drain-source voltage; typical values



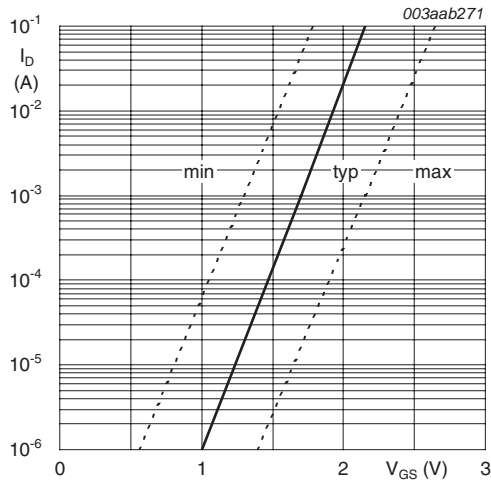
$V_{DS} > I_D \times R_{DSon}$

Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values



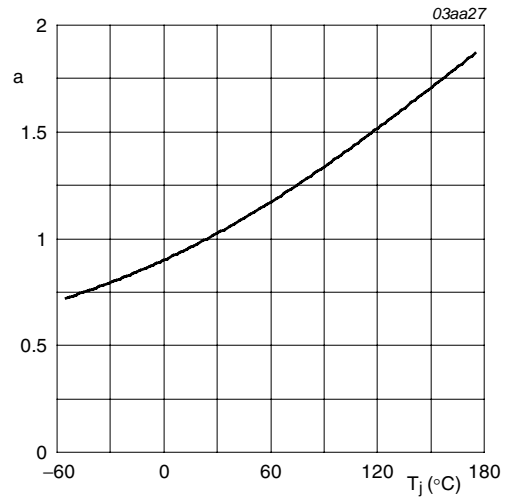
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature



$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 5\text{ V}$

Fig 11. Sub-threshold drain current as a function of gate-source voltage



$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

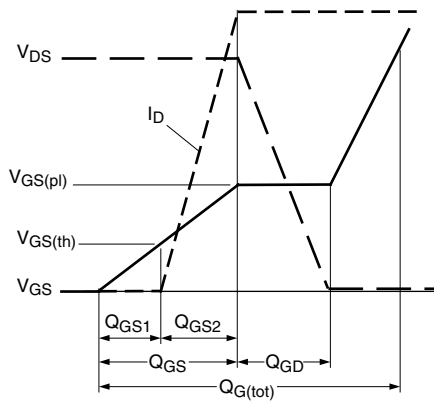
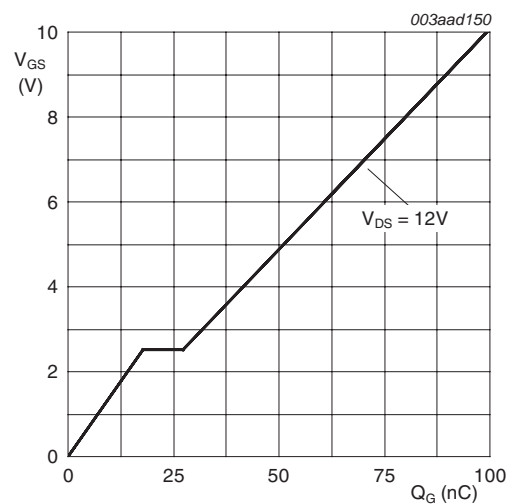
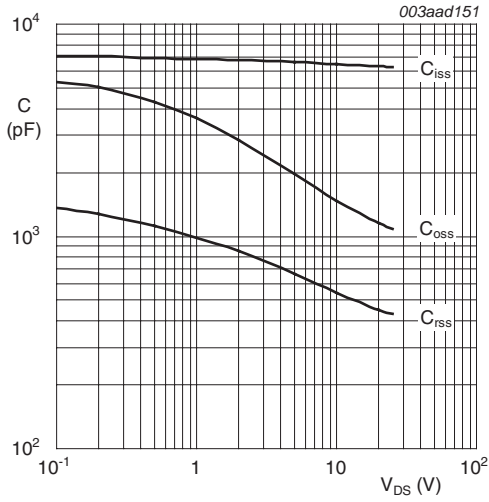


Fig 13. Gate charge waveform definitions



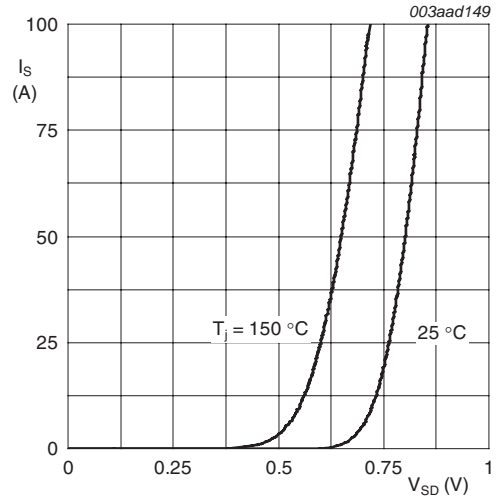
$I_D = 25\text{ A}$

Fig 14. Gate-source voltage as a function of gate charge; typical values



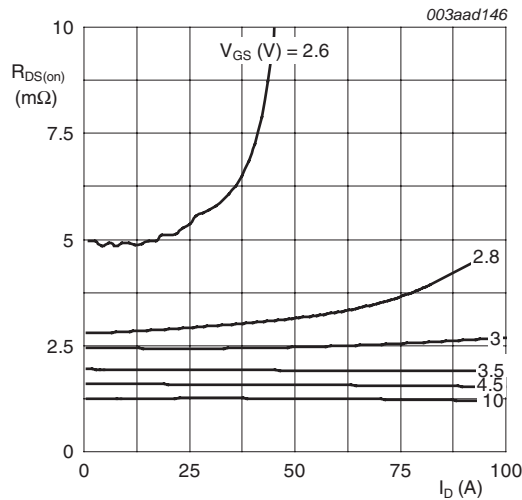
$V_{GS} = 0V; f = 1MHz$

Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0V$

Fig 16. Source current as a function of source-drain voltage; typical values



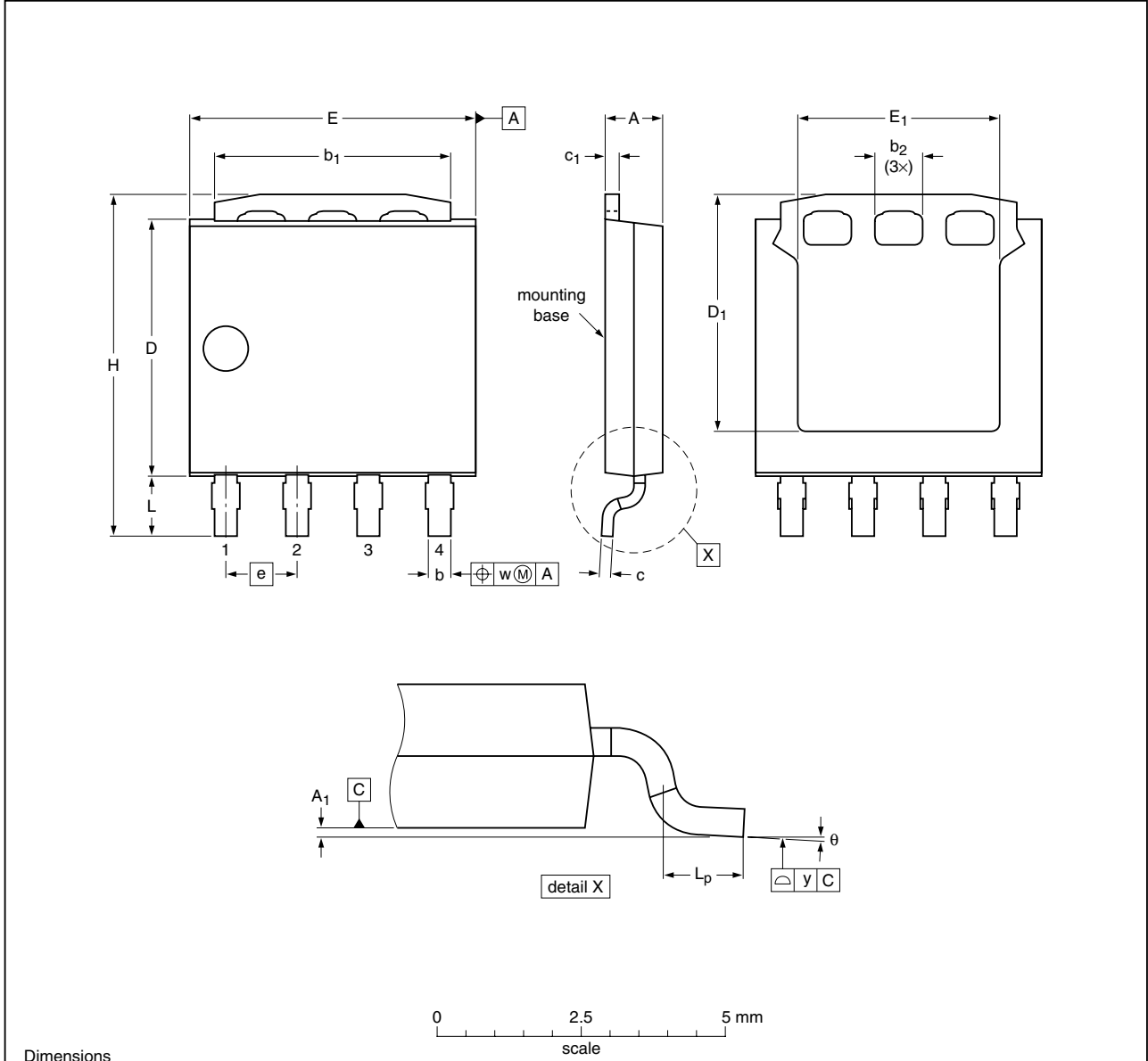
$T_j = 25 °C$

Fig 17. Drain-source on-state resistance as a function of drain current; typical values

7. Package outline

Plastic single-ended surface-mounted package (LPAK2); 4 leads

SOT1023



Dimensions

Unit	A	A ₁	b	b ₁	b ₂	c	c ₁	D ⁽¹⁾	D ₁ ⁽¹⁾	E ⁽¹⁾	E ₁ ⁽¹⁾	e	H	L	L _p	w	y	θ
max	1.10	0.15	0.50	4.41		0.25	0.30	4.70	4.45	5.30	3.7		6.2	1.3	0.85			8°
nom				0.85								1.27				0.25	0.1	
min	0.95	0.00	0.35	3.62		0.19	0.24	4.45		4.95	3.5		5.9	0.8	0.40			0°

Note

1. Plastic or metal protrusions of 0.15 mm per side are not included.

sot1023_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1023					08-10-13 09-05-26

Fig 18. Package outline SOT1023; Package outline

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN1R3-30YL_2	20090625	Product data sheet	-	PSMN2R3-30YL_1
Modifications:		<ul style="list-style-type: none">• Status changed from objective to product.• Various changes to content.		
PSMN1R3-30YL_1	20090528	Objective data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at <http://www.nxp.com>.

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11. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	2
3	Ordering information	2
4	Limiting values	3
5	Thermal characteristics	5
6	Characteristics	6
7	Package outline	11
8	Revision history	12
9	Legal information	13
9.1	Data sheet status	13
9.2	Definitions	13
9.3	Disclaimers	13
9.4	Trademarks	13
10	Contact information	13

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