

# PSMN038-100K

## N-channel TrenchMOS SiliconMAX standard level FET

Rev. 02 — 25 November 2009

Product data sheet

## 1. Product profile

### 1.1 General description

SiliconMAX standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for high frequency applications due to fast switching characteristics

### 1.3 Applications

- Computer motherboards
- DC-to-DC convertors
- Switched-mode power supplies

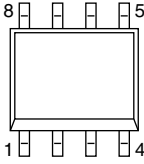
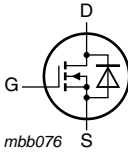
### 1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 150\text{ °C}$	-	-	100	V
$I_D$	drain current	$T_{sp} = 80\text{ °C};$ see <a href="#">Figure 1</a> and <a href="#">3</a>	-	-	6.3	A
$P_{tot}$	total power dissipation	$T_{sp} = 80\text{ °C};$ see <a href="#">Figure 2</a>	-	-	3.5	W
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 6.3\text{ A};$ $V_{DS} = 50\text{ V}; T_j = 25\text{ °C};$ see <a href="#">Figure 11</a>	-	16	21.5	nC
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 5.2\text{ A};$ $T_j = 25\text{ °C};$ see <a href="#">Figure 9</a> and <a href="#">10</a>	-	33	38	m $\Omega$

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>SOT96-1 (SO8)</p>	
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

## 3. Ordering information

Table 3. Ordering information

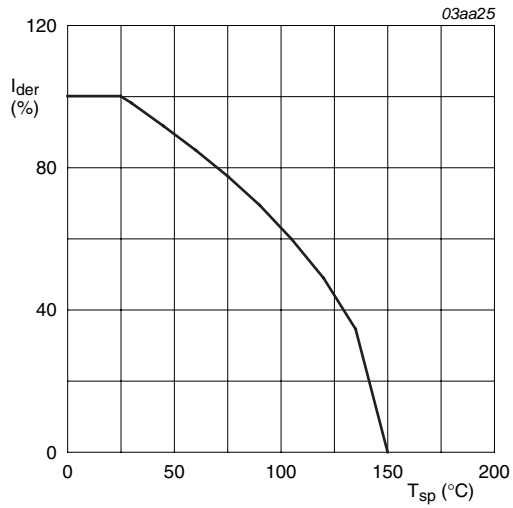
Type number	Package		
	Name	Description	Version
PSMN038-100K	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

## 4. Limiting values

Table 4. Limiting values

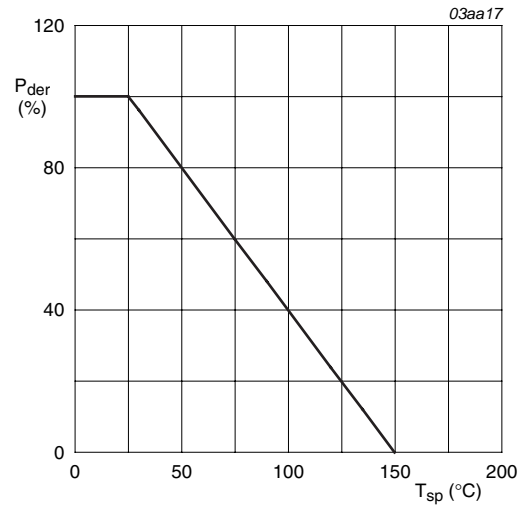
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	100	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$T_{sp} = 80\text{ °C}$ ; see <a href="#">Figure 1</a> and <a href="#">3</a>	-	6.3	A
$I_{DM}$	peak drain current	$T_{sp} = 25\text{ °C}$ ; $t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; see <a href="#">Figure 3</a>	-	50	A
$P_{tot}$	total power dissipation	$T_{sp} = 80\text{ °C}$ ; see <a href="#">Figure 2</a>	-	3.5	W
$T_{stg}$	storage temperature		-55	150	°C
$T_j$	junction temperature		-55	150	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{sp} = 80\text{ °C}$	-	3.1	A
$I_{SM}$	peak source current	$T_{sp} = 25\text{ °C}$ ; $t_p \leq 10\text{ }\mu\text{s}$ ; pulsed	-	50	A



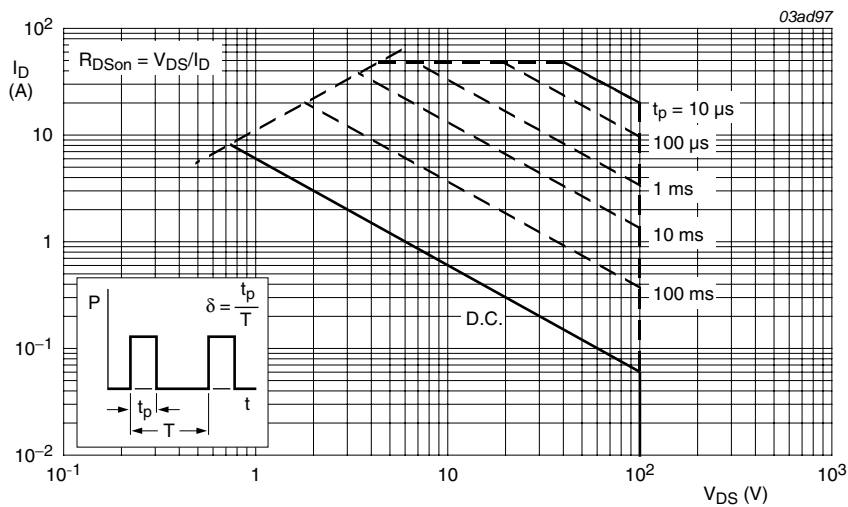
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of solder point temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature



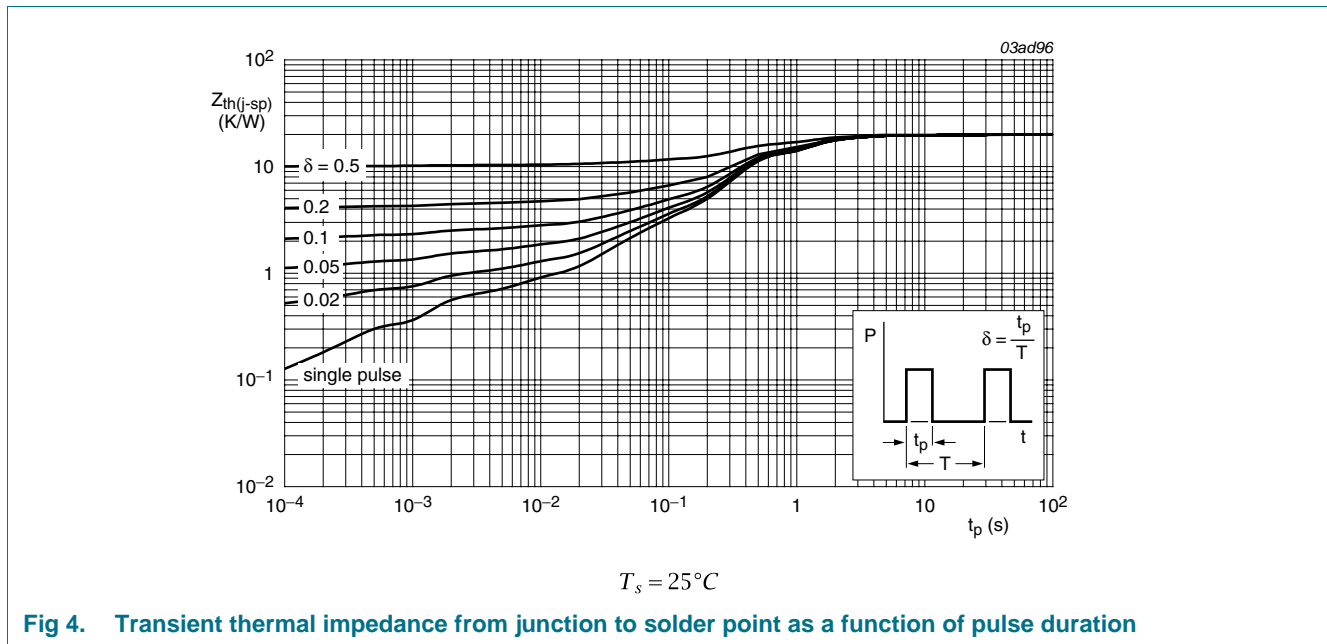
$T_{sp} = 25^\circ\text{C}; I_{DM}$  is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

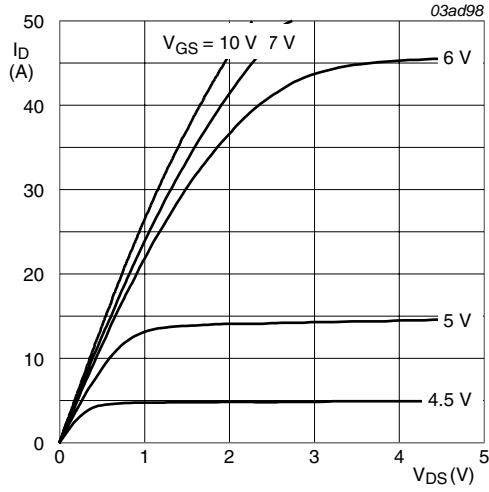
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	mounted on a metal clad substrate; see <a href="#">Figure 4</a>	-	-	20	K/W



## 6. Characteristics

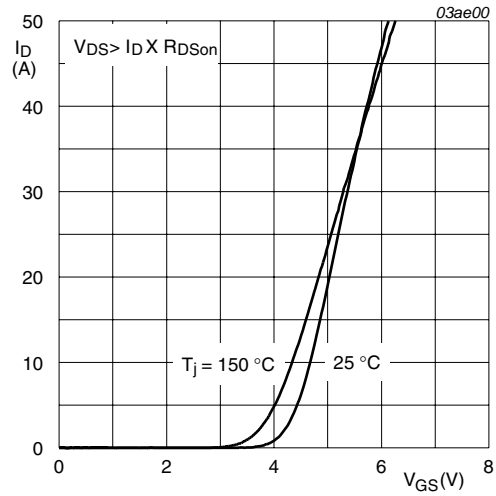
**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	100	130	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 150 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 8</a>	1.2	-	-	V
		$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = -55 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 8</a>	-	-	6	V
		$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 8</a>	2	-	4	V
$I_{DSS}$	drain leakage current	$V_{DS} = 100 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 150 \text{ }^\circ\text{C}$	-	-	0.5	mA
		$V_{DS} = 80 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	1	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -20 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}$ ; $I_D = 5.2 \text{ A}$ ; $T_j = 150 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 9</a> and <a href="#">10</a>	-	76	88	m $\Omega$
		$V_{GS} = 10 \text{ V}$ ; $I_D = 5.2 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 9</a> and <a href="#">10</a>	-	33	38	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 6.3 \text{ A}$ ; $V_{DS} = 50 \text{ V}$ ; $V_{GS} = 10 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 11</a>	-	43	-	nC
$Q_{GS}$	gate-source charge		-	6.5	-	nC
$Q_{GD}$	gate-drain charge		-	16	21.5	nC
$C_{iss}$	input capacitance	$V_{DS} = 25 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $f = 1 \text{ MHz}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 12</a>	-	1740	-	pF
$C_{oss}$	output capacitance		-	220	-	pF
$C_{rss}$	reverse transfer capacitance		-	135	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 50 \text{ V}$ ; $R_L = 50 \text{ }^\circ\Omega$ ; $V_{GS} = 10 \text{ V}$ ; $R_{G(ext)} = 6 \text{ }^\circ\Omega$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; $I_D = 1 \text{ A}$	-	15	30	ns
$t_r$	rise time		-	13	25	ns
$t_{d(off)}$	turn-off delay time		-	50	80	ns
$t_f$	fall time		-	25	40	ns
$g_{fs}$	transfer conductance	$V_{DS} = 15 \text{ V}$ ; $I_D = 6.3 \text{ A}$ ; see <a href="#">Figure 13</a>	-	20	-	S
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 2.3 \text{ A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 14</a>	-	0.7	1.1	V
$t_{rr}$	reverse recovery time	$I_S = 6.3 \text{ A}$ ; $di_S/dt = -100 \text{ A}/\mu\text{s}$ ; $V_{GS} = 0 \text{ V}$ ; $V_{DS} = 25 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	85	-	ns
$Q_r$	recovered charge		-	0.3	-	$\mu\text{C}$



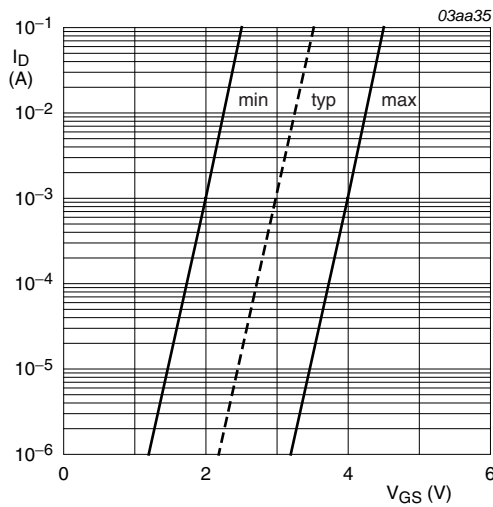
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



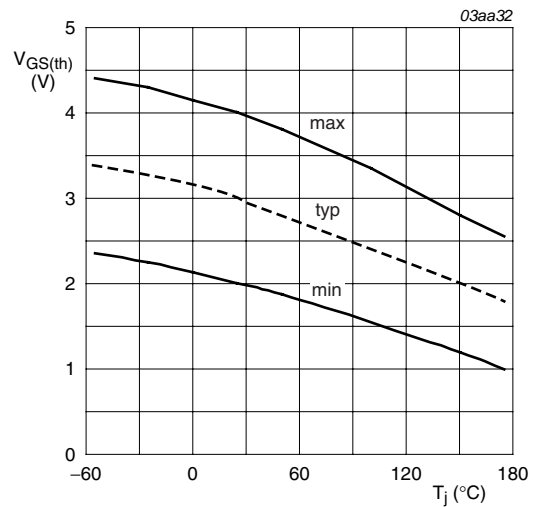
$T_j = 25^\circ\text{C}$  and  $150^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



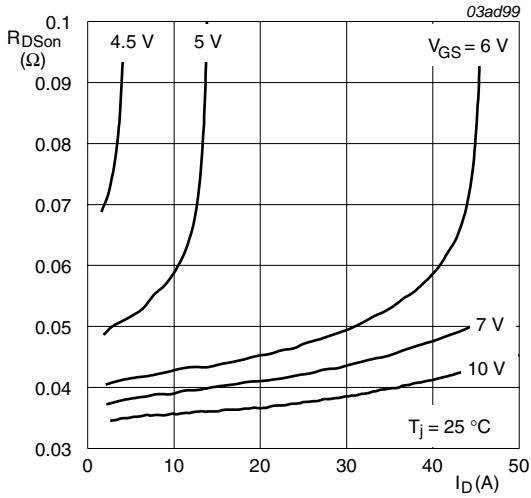
$T_j = 25^\circ\text{C}$ ;  $V_{DS} = 5\text{V}$

Fig 7. Sub-threshold drain current as a function of gate-source voltage



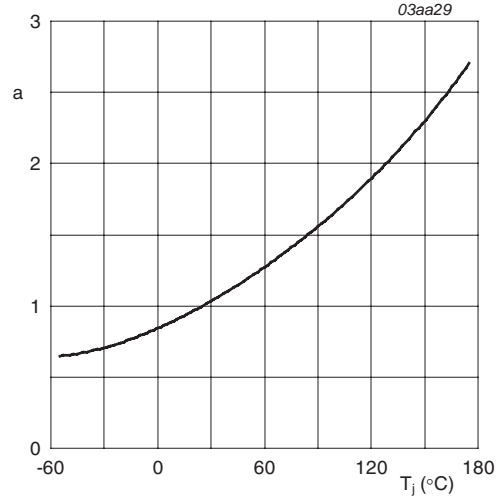
$I_D = 1\text{mA}$ ;  $V_{DS} = V_{GS}$

Fig 8. Gate-source threshold voltage as a function of junction temperature



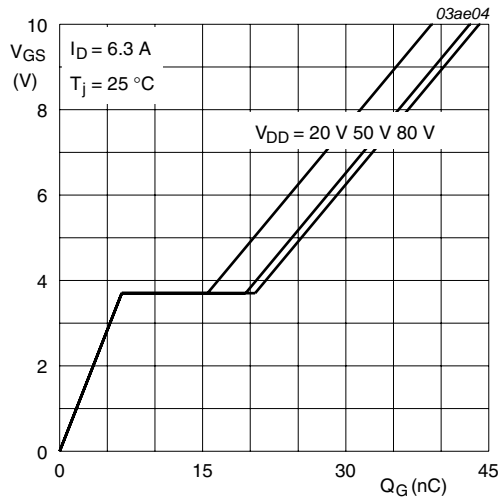
$T_j = 25^\circ\text{C}$

Fig 9. Drain-source on-state resistance as a function of drain current; typical values



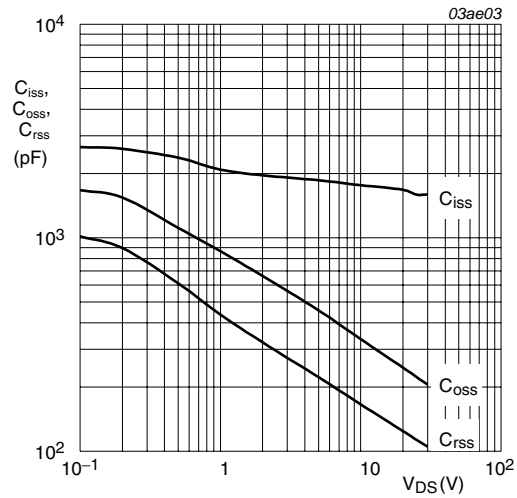
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



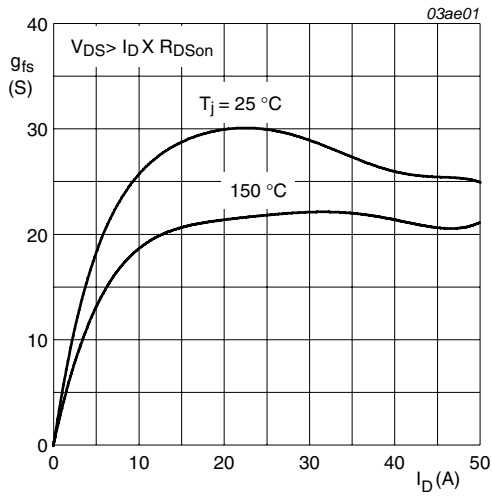
$I_D = 6.3\text{ A}; V_{DS} = 20\text{ V}, 50\text{ V and } 80\text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values



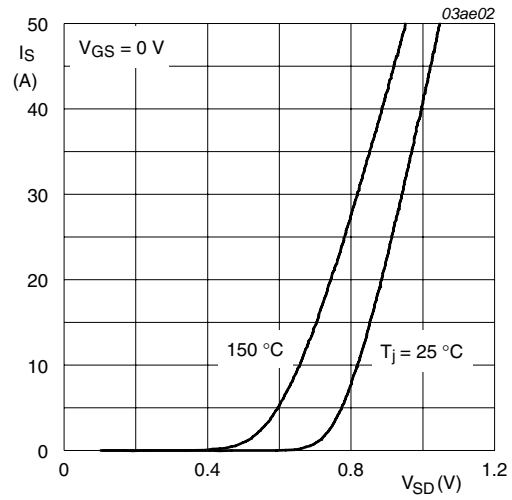
$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25\text{ }^\circ\text{C}$  and  $150\text{ }^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

**Fig 13. Forward transconductance as a function of drain current; typical values**



$T_j = 25\text{ }^\circ\text{C}$  and  $150\text{ }^\circ\text{C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 14. Source current as a function of source-drain voltage; typical values**



7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

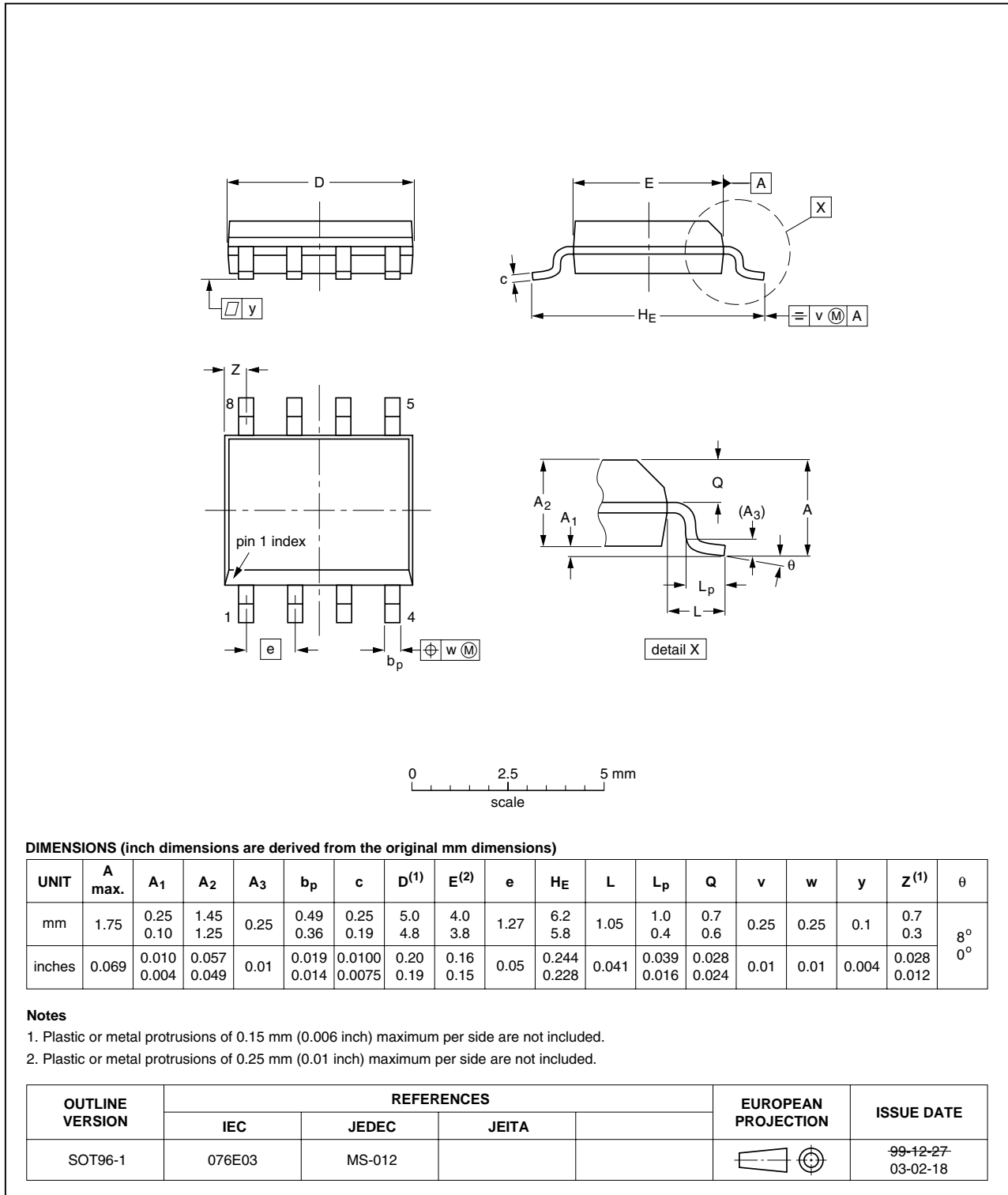


Fig 15. Package outline SOT96-1 (SO8)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN038-100K_2	20091125	Product data sheet	-	PSMN038-100K-01
Modifications:				
				<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li></ul>
PSMN038-100K-01	20010116	Product specification	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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