

# PMK30EP

## P-channel TrenchMOS extremely low level FET

Rev. 04 — 25 October 2010

Product data sheet

## 1. Product profile

### 1.1 General description

Extremely low level P-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance

### 1.3 Applications

- Battery management
- Load switching

### 1.4 Quick reference data

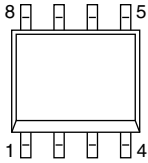
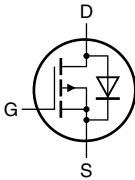
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-	-30	V
$I_D$	drain current	$T_{sp} = 25\text{ °C}$ ; $V_{GS} = -10\text{ V}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	-	-14.9	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	6.9	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -10\text{ V}$ ; $I_D = -9.2\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 9</a>	-	16	19	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = -10\text{ V}$ ; $I_D = -9.2\text{ A}$ ; $V_{DS} = -15\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	-	7	-	nC



## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>SOT96-1 (SO8)</p>	 <p>001aaa025</p>
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMK30EP	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

## 4. Limiting values

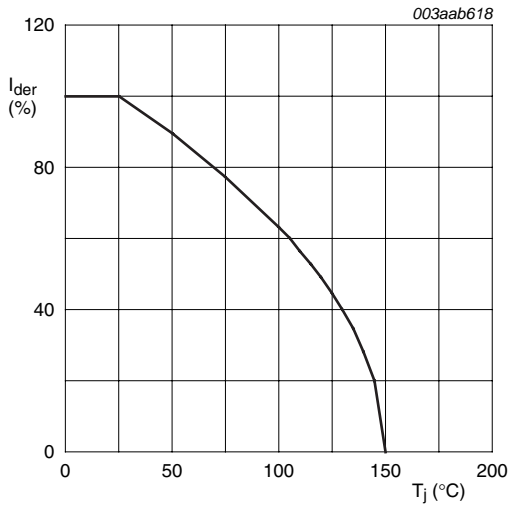
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-30	V
$V_{DGR}$	drain-gate voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	-30	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$T_{sp} = 25\text{ °C}$ ; $V_{GS} = -10\text{ V}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	-14.9	A
		$T_{sp} = 100\text{ °C}$ ; $V_{GS} = -10\text{ V}$ ; see <a href="#">Figure 1</a>	-	-7.5	A
$I_{DM}$	peak drain current	$T_{sp} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; see <a href="#">Figure 3</a>	-	-28.8	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	6.9	W
$T_{stg}$	storage temperature		-55	150	°C
$T_j$	junction temperature		-55	150	°C

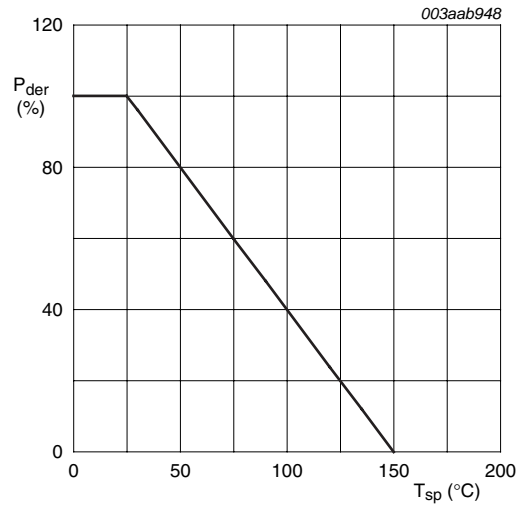
### Source-drain diode

$I_S$	source current	$T_{sp} = 25\text{ °C}$	-	-5.8	A
$I_{SM}$	peak source current	$T_{sp} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	-23	A



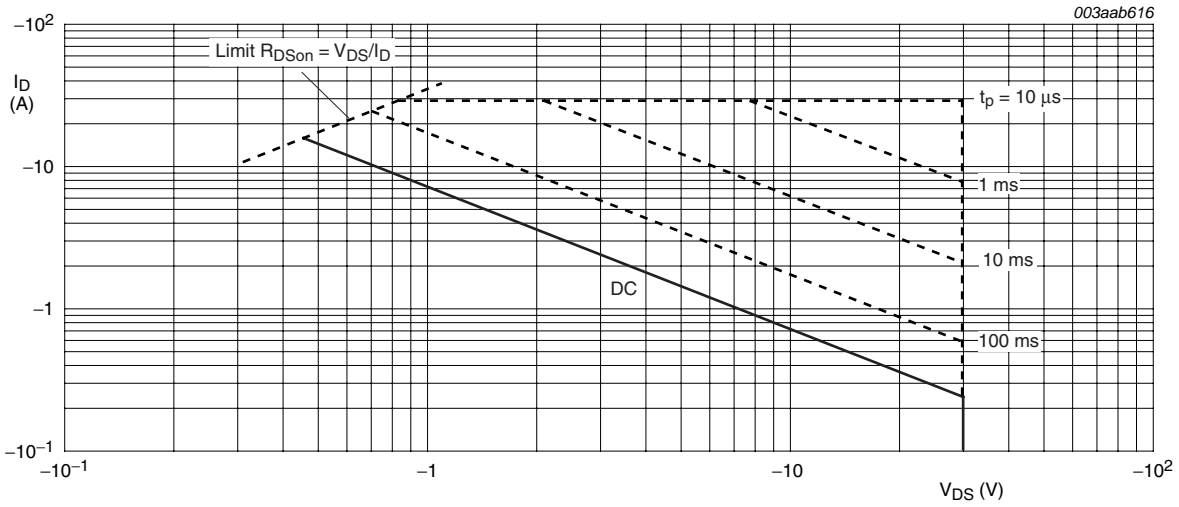
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100 \%$$

Fig 1. Normalized continuous drain current as a function of solder point temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100 \%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature



$T_{sp} = 25^\circ\text{C}$ ;  $I_{DM}$  is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

### 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see <a href="#">Figure 4</a>	-	-	18	K/W

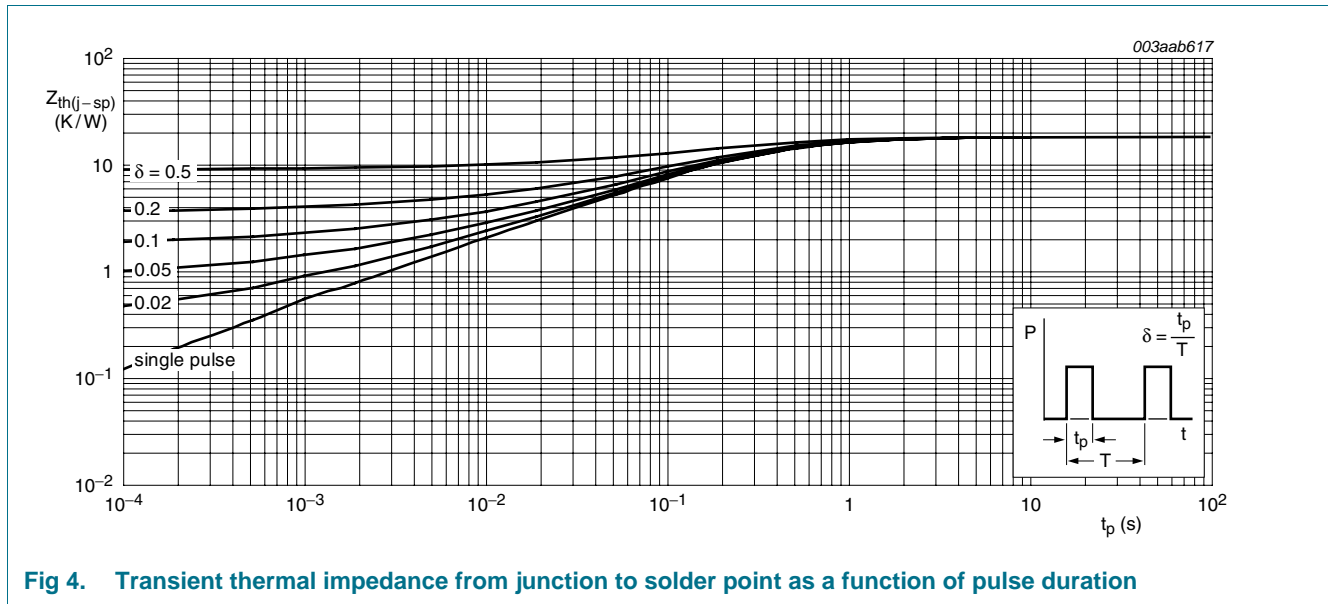
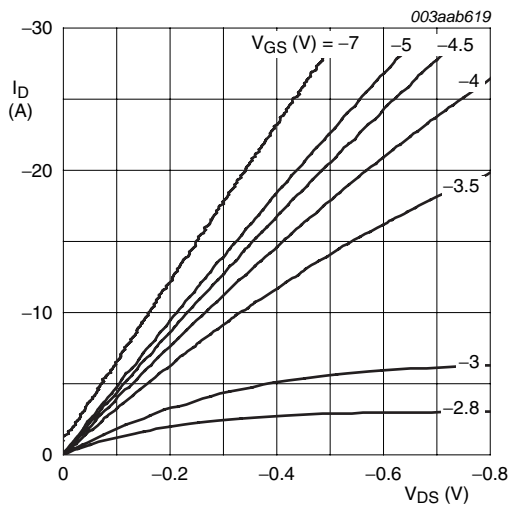


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

## 6. Characteristics

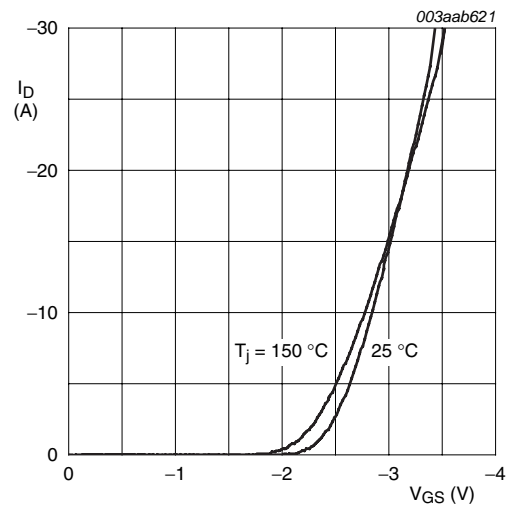
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-30	-	-	V
		$I_D = -250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	-27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	-1	-	-3	V
		$I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ C$ ; see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	-0.7	-	-	V
		$I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$ ; see <a href="#">Figure 7</a> ; see <a href="#">Figure 8</a>	-	-	-3.3	V
$I_{DSS}$	drain leakage current	$V_{DS} = -30 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-1	$\mu A$
		$V_{DS} = -30 V; V_{GS} = 0 V; T_j = 70 \text{ }^\circ C$	-	-	-10	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-100	nA
		$V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -10 V; I_D = -9.2 A; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 9</a>	-	16	19	m $\Omega$
		$V_{GS} = -10 V; I_D = -9.2 A; T_j = 150 \text{ }^\circ C$ ; see <a href="#">Figure 9</a>	-	25	31	m $\Omega$
		$V_{GS} = -4.5 V; I_D = -7.3 A; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 10</a> ; see <a href="#">Figure 9</a>	-	24	30	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = -9.2 A; V_{DS} = -15 V; V_{GS} = -10 V; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	-	50	-	nC
$Q_{GS}$	gate-source charge	$I_D = -9.2 A; V_{DS} = -15 V; V_{GS} = -10 V$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	-	7	-	nC
$Q_{GD}$	gate-drain charge	$I_D = -9.2 A; V_{DS} = -15 V; V_{GS} = -10 V; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	-	7	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = -9.2 A; V_{DS} = -15 V; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	-	-2.5	-	V
$C_{iss}$	input capacitance	$V_{DS} = -25 V; V_{GS} = 0 V; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 13</a>	-	2240	-	pF
$C_{oss}$	output capacitance		-	325	-	pF
$C_{riss}$	reverse transfer capacitance		-	220	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -15 V; R_L = 6 \Omega; V_{GS} = -10 V; R_{G(ext)} = 6 \Omega; T_j = 25 \text{ }^\circ C$	-	10	-	ns
$t_r$	rise time		-	8	-	ns
$t_{d(off)}$	turn-off delay time		-	56	-	ns
$t_f$	fall time		-	21	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = -3.45 A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 14</a>	-	-0.8	-1.2	V



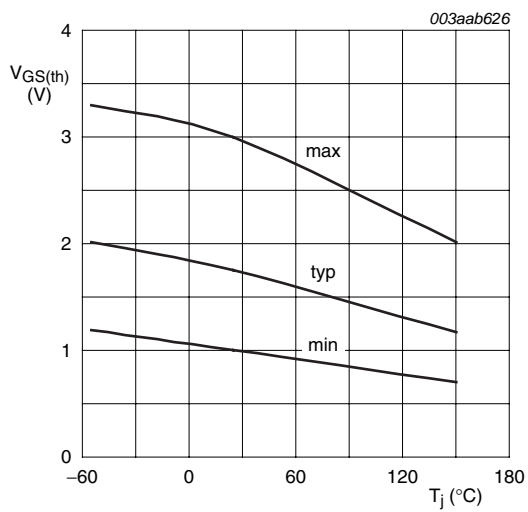
$T_j = 25\text{ °C}$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



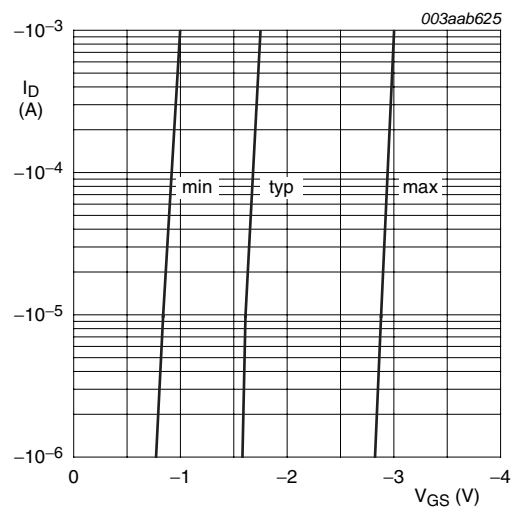
$V_{DS} > I_D \times R_{DSon}$

**Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



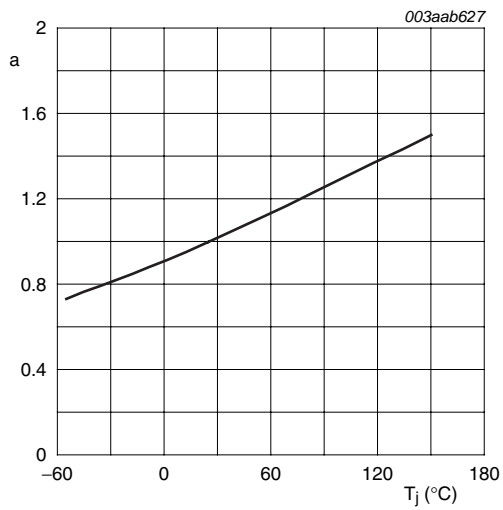
$I_D = -1\text{ mA}; V_{DS} = V_{GS}$

**Fig 7. Gate-source threshold voltage as a function of junction temperature**



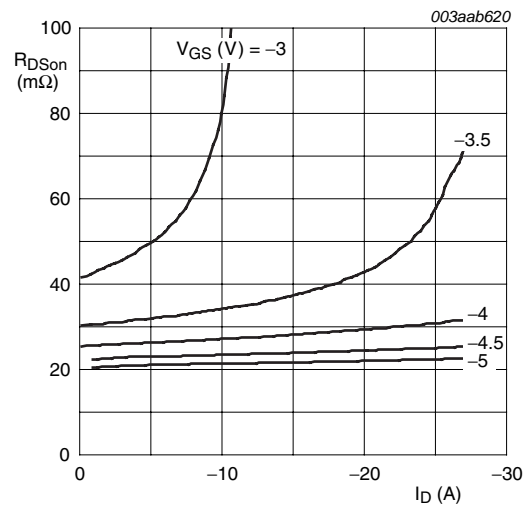
$T_j = 25\text{ °C}; V_{DS} = -5\text{ V}$

**Fig 8. Sub-threshold drain current as a function of gate-source voltage**



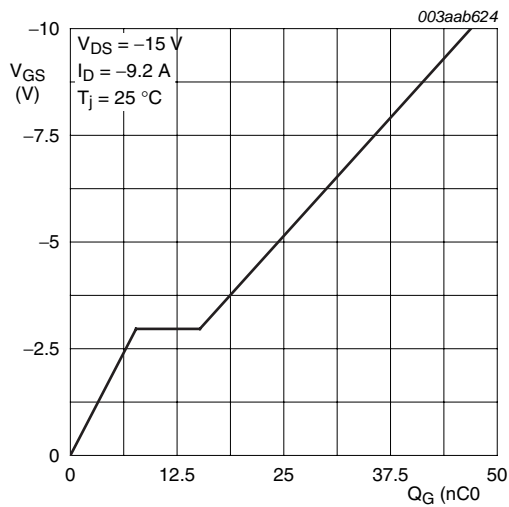
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature



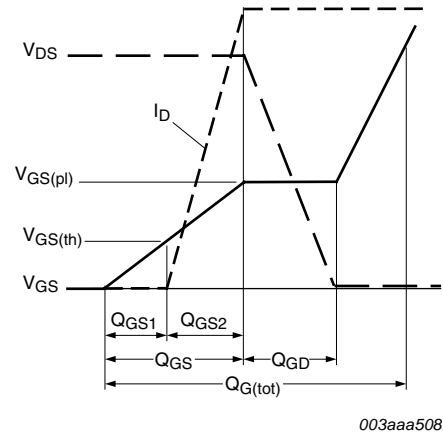
T<sub>j</sub> = 25 °C

Fig 10. Drain-source on-state resistance as a function of drain current; typical values



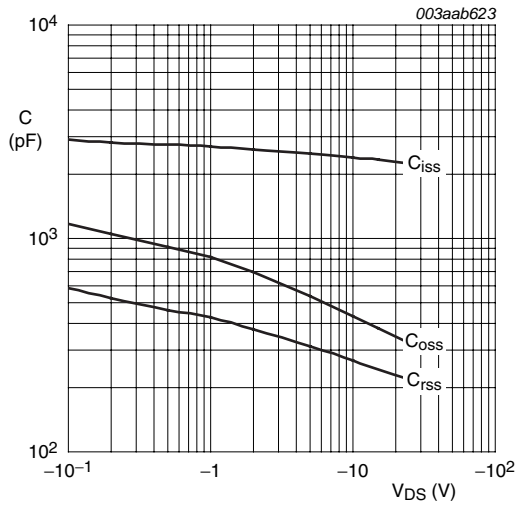
V<sub>DS</sub> = -15 V; I<sub>D</sub> = -9.2 A; T<sub>j</sub> = 25 °C

Fig 11. Gate-source voltage as a function of gate charge; typical values



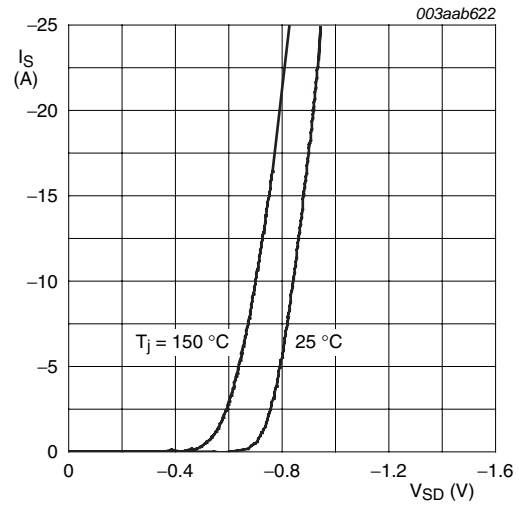
003aaa508

Fig 12. Gate charge waveform definitions



V<sub>GS</sub> = 0 V; f = 1 MHz

**Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



V<sub>GS</sub> = 0 V

**Fig 14. Source current as a function of source-drain voltage; typical values**



7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

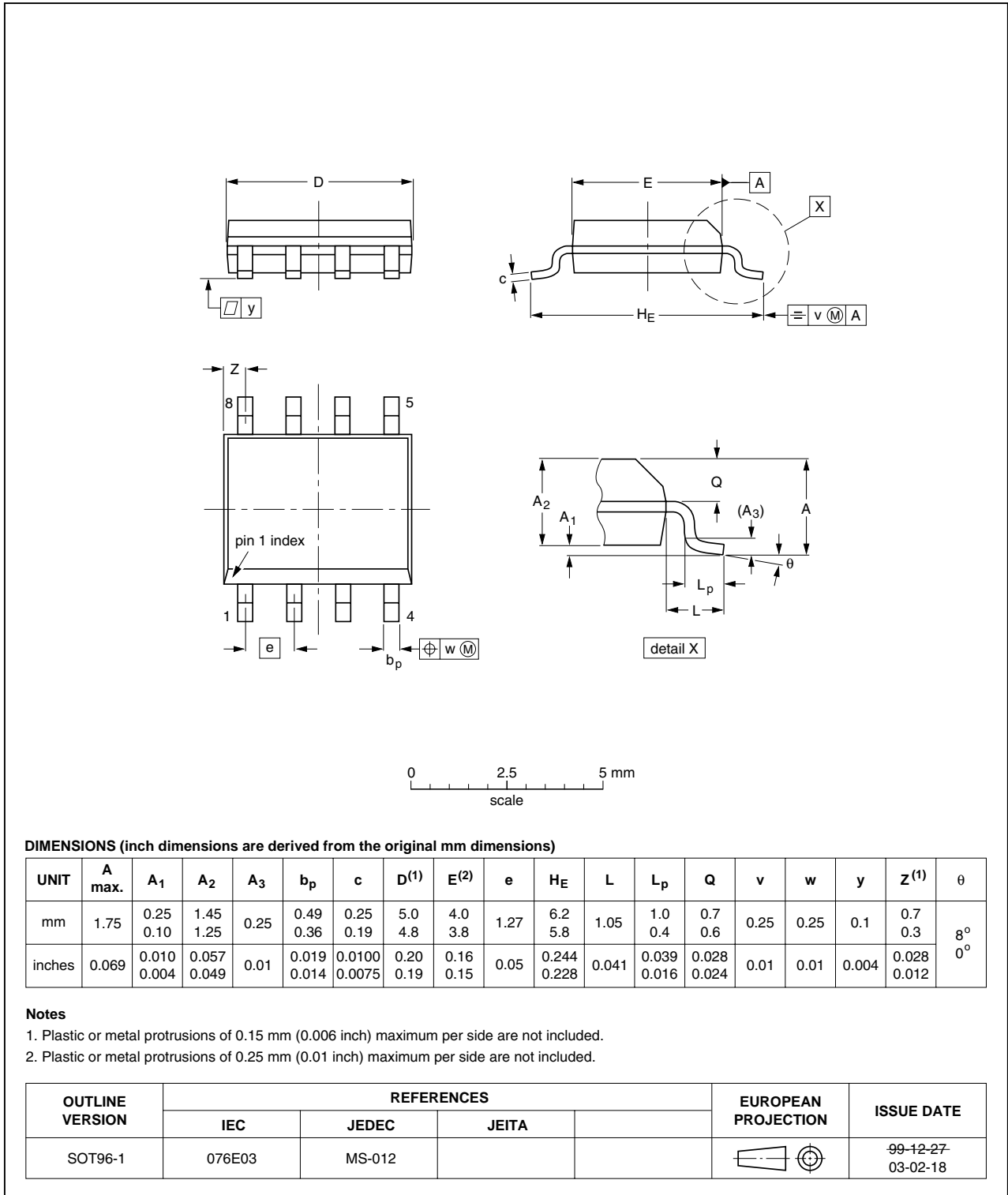


Fig 15. Package outline SOT96-1 (SO8)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMK30EP v.4	20101025	Product data sheet	-	PMK30EP v.3
Modifications:	• Various changes to content.			
PMK30EP v.3	20100429	Product data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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