

# PMF3800SN

## N-channel TrenchMOS standard level FET

Rev. 03 — 11 November 2009

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Electrostatically robust due to integrated protection diodes
- Saves PCB space due to small footprint
- Suitable for high frequency applications due to fast switching characteristics
- Suitable for logic level gate drive sources

### 1.3 Applications

- High-speed line drivers
- Relay drivers

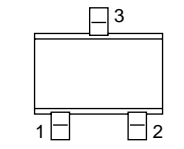
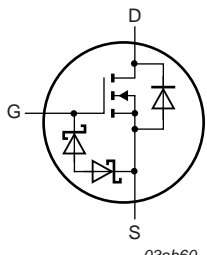
### 1.4 Quick reference data

Table 1. Quick reference

| Symbol                         | Parameter                        | Conditions   | Min | Typ  | Max  | Unit     |
|--------------------------------|----------------------------------|--|-----|------|------|----------|
| $V_{DS}$                       | drain-source voltage             | $T_j \geq 25\text{ °C}; T_j \leq 150\text{ °C}$  | -   | -    | 60   | V        |
| $I_D$                          | drain current                    | $T_{sp} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see <a href="#">Figure 1</a> and <a href="#">3</a>                          | -   | -    | 260  | mA       |
| $P_{tot}$                      | total power dissipation          | $T_{sp} = 25\text{ °C};$ see <a href="#">Figure 2</a>  | -   | -    | 0.56 | W        |
| <b>Dynamic characteristics</b> |                                  |  |     |      |      |          |
| $Q_{GD}$                       | gate-drain charge                | $V_{GS} = 10\text{ V}; I_D = 0.5\text{ A};$  | -   | 0.07 | -    | nC       |
| $Q_{G(tot)}$                   | total gate charge                | $V_{DS} = 48\text{ V}; T_j = 25\text{ °C};$ see <a href="#">Figure 11</a>  | -   | 0.85 | -    | nC       |
| <b>Static characteristics</b>  |                                  |  |     |      |      |          |
| $R_{DS(on)}$                   | drain-source on-state resistance | $V_{GS} = 4.5\text{ V}; I_D = 200\text{ mA};$<br>$T_j = 25\text{ °C};$ see <a href="#">Figure 9</a> and <a href="#">10</a> | -   | 3.8  | 5.3  | $\Omega$ |
|                                |                                  | $V_{GS} = 10\text{ V}; I_D = 500\text{ mA};$<br>$T_j = 25\text{ °C};$ see <a href="#">Figure 9</a> and <a href="#">10</a>  | -   | 2.8  | 4.5  | $\Omega$ |

## 2. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline   | Graphic symbol  |
|-----|--------|-------------|--|---|
| 1   | G      | gate        |  <p>SOT323 (SC-70)</p> |  <p>03ab60</p> |
| 2   | S      | source      |  |   |
| 3   | D      | drain       |  |   |

## 3. Ordering information

Table 3. Ordering information

| Type number | Package |  | Version |
|-------------|---------|--|---------|
|             | Name    | Description                              |         |
| PMF3800SN   | SC-70   | plastic surface-mounted package; 3 leads | SOT323  |

## 4. Marking

Table 4. Marking codes

| Type number | Marking code <sup>[1]</sup> |
|-------------|-----------------------------|
| PMF3800SN   | FK*                         |

- [1] \* = -: made in Hong Kong  
 \* = p: made in Hong Kong  
 \* = t: made in Malaysia  
 \* = W: made in China

## 5. Limiting values

Table 5. Limiting values

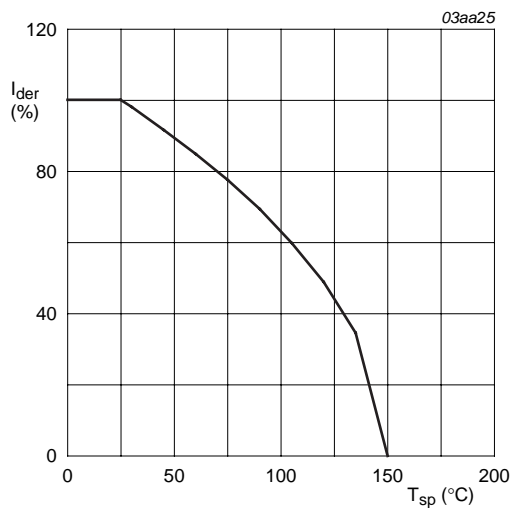
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol    | Parameter               | Conditions  | Min | Max  | Unit |
|-----------|-------------------------|---|-----|------|------|
| $V_{DS}$  | drain-source voltage    | $T_j \geq 25\text{ °C}; T_j \leq 150\text{ °C}$   | -   | 60   | V    |
| $V_{DGR}$ | drain-gate voltage      | $T_j \geq 25\text{ °C}; T_j \leq 150\text{ °C}; R_{GS} = 20\text{ k}\Omega$                       | -   | 60   | V    |
| $V_{GS}$  | gate-source voltage     |   | -15 | 15   | V    |
| $I_D$     | drain current           | $T_{sp} = 100\text{ °C}; V_{GS} = 10\text{ V};$ see <a href="#">Figure 1</a>                      | -   | 165  | mA   |
|           |                         | $T_{sp} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see <a href="#">Figure 1</a> and <a href="#">3</a> | -   | 260  | mA   |
| $I_{DM}$  | peak drain current      | $T_{sp} = 25\text{ °C}; t_p \leq 10\text{ }\mu\text{s};$ pulsed; see <a href="#">Figure 3</a>     | -   | 560  | mA   |
| $P_{tot}$ | total power dissipation | $T_{sp} = 25\text{ °C};$ see <a href="#">Figure 2</a>   | -   | 0.56 | W    |
| $T_{stg}$ | storage temperature     |   | -55 | 150  | °C   |
| $T_j$     | junction temperature    |   | -55 | 150  | °C   |

**Table 5. Limiting values ...continued**

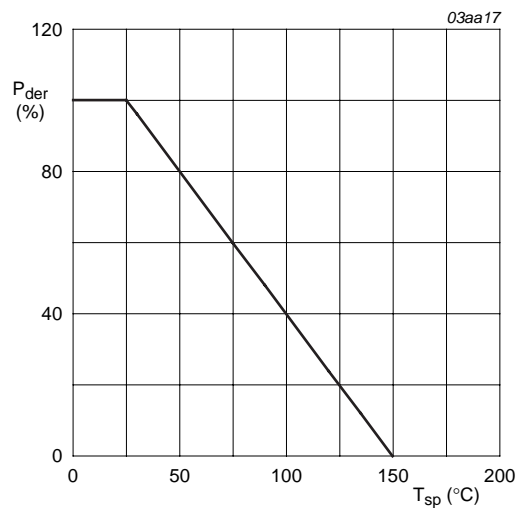
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol                                 | Parameter                       | Conditions  | Min | Max | Unit |
|--|---------------------------------|---|-----|-----|------|
| <b>Source-drain diode</b>              |                                 |   |     |     |      |
| $I_S$                                  | source current                  | $T_{sp} = 25\text{ }^\circ\text{C}$   | -   | 280 | mA   |
| $I_{SM}$                               | peak source current             | $T_{sp} = 25\text{ }^\circ\text{C}$ ; $t_p \leq 10\text{ }\mu\text{s}$ ; pulsed | -   | 560 | mA   |
| <b>Electrostatic discharge voltage</b> |                                 |   |     |     |      |
| $V_{ESD}$                              | electrostatic discharge voltage | HBM; C = 100 pF; R = 1.5 k $\Omega$   | -   | 1   | kV   |



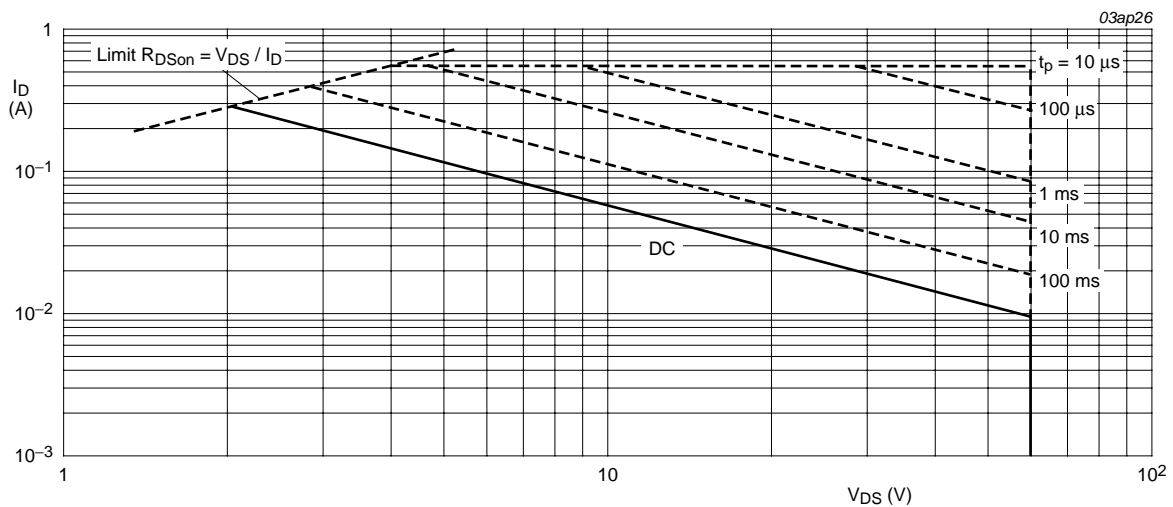
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

**Fig 1. Normalized continuous drain current as a function of solder point temperature**



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

**Fig 2. Normalized total power dissipation as a function of solder point temperature**



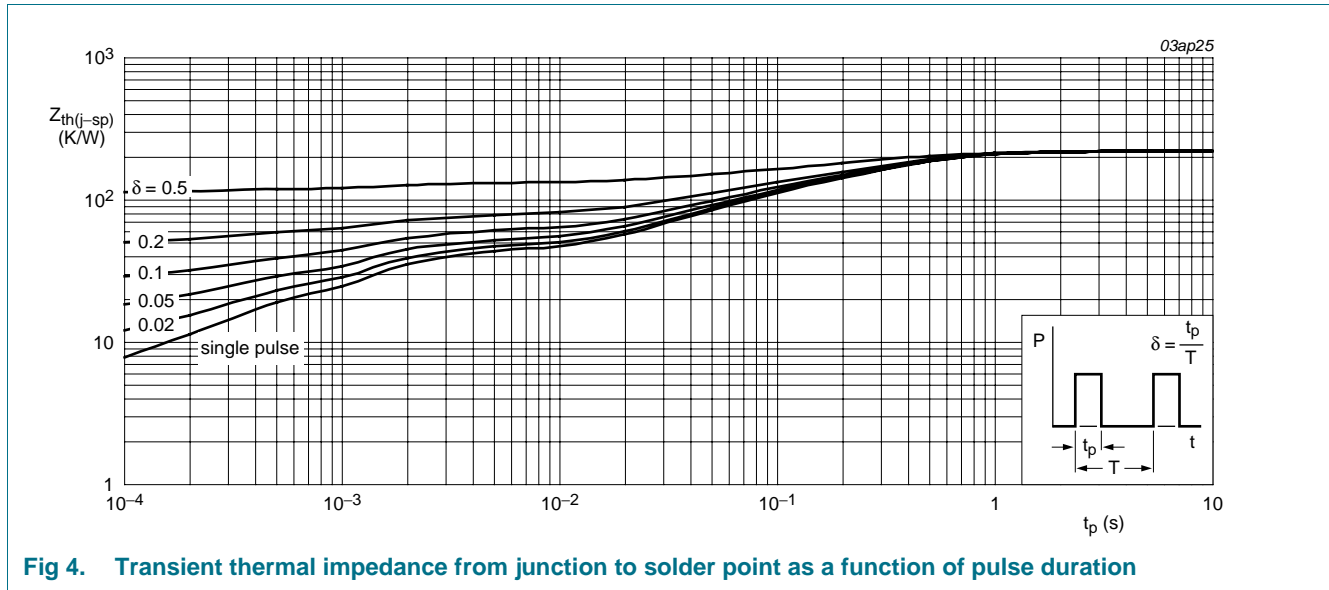
$T_{sp} = 25\text{ }^\circ\text{C}$ ;  $I_{DM}$  is single pulse

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

## 6. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol         | Parameter  | Conditions                   | Min | Typ | Max | Unit |
|----------------|--|------------------------------|-----|-----|-----|------|
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | see <a href="#">Figure 4</a> | -   | -   | 220 | K/W  |

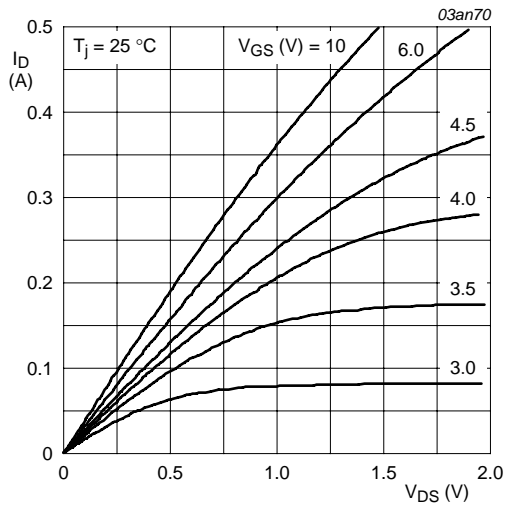


**Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration**

## 7. Characteristics

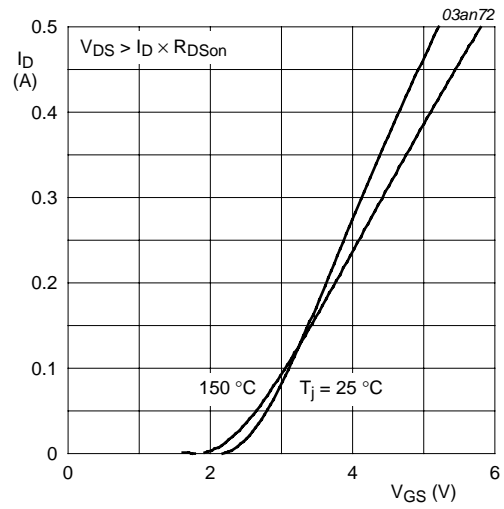
**Table 7. Characteristics**

| Symbol                         | Parameter                        | Conditions   | Min | Typ  | Max | Unit          |
|--------------------------------|----------------------------------|--|-----|------|-----|---------------|
| <b>Static characteristics</b>  |                                  |  |     |      |     |               |
| $V_{(BR)DSS}$                  | drain-source breakdown voltage   | $I_D = 10 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$   | 55  | -    | -   | V             |
|                                |                                  | $I_D = 10 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$  | 60  | -    | -   | V             |
| $V_{GS(th)}$                   | gate-source threshold voltage    | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 7</a> and <a href="#">8</a>   | 0.6 | -    | -   | V             |
|                                |                                  | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 7</a> and <a href="#">8</a>   | -   | -    | 3.5 | V             |
|                                |                                  | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 7</a> and <a href="#">8</a>  | 1   | 2    | 3.3 | V             |
| $I_{DSS}$                      | drain leakage current            | $V_{DS} = 48 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$   | -   | -    | 1   | $\mu\text{A}$ |
|                                |                                  | $V_{DS} = 48 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$  | -   | -    | 10  | $\mu\text{A}$ |
| $I_{GSS}$                      | gate leakage current             | $V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$  | -   | 50   | 500 | nA            |
|                                |                                  | $V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$   | -   | 50   | 500 | nA            |
| $R_{DS(on)}$                   | drain-source on-state resistance | $V_{GS} = 10 \text{ V}; I_D = 500 \text{ mA}; T_j = 150 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 9</a> and <a href="#">10</a>                                    | -   | 5.2  | 8.4 | $\Omega$      |
|                                |                                  | $V_{GS} = 4.5 \text{ V}; I_D = 200 \text{ mA}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 9</a> and <a href="#">10</a>                                    | -   | 3.8  | 5.3 | $\Omega$      |
|                                |                                  | $V_{GS} = 10 \text{ V}; I_D = 500 \text{ mA}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 9</a> and <a href="#">10</a>                                     | -   | 2.8  | 4.5 | $\Omega$      |
| $V_{(BR)GSS}$                  | gate-source breakdown voltage    | $V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}; I_G = -1 \text{ mA}$   | 16  | 22   | -   | V             |
|                                |                                  | $T_j = 25 \text{ }^\circ\text{C}; I_G = 1 \text{ mA}; V_{DS} = 0 \text{ V}$  | 16  | 22   | -   | V             |
| <b>Dynamic characteristics</b> |                                  |  |     |      |     |               |
| $Q_{G(tot)}$                   | total gate charge                | $I_D = 0.5 \text{ A}; V_{DS} = 48 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 11</a>                                     | -   | 0.85 | -   | nC            |
| $Q_{GS}$                       | gate-source charge               |  | -   | 0.55 | -   | nC            |
| $Q_{GD}$                       | gate-drain charge                |  | -   | 0.07 | -   | nC            |
| $C_{iss}$                      | input capacitance                | $V_{DS} = 10 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 12</a>  | -   | 13   | 40  | pF            |
| $C_{oss}$                      | output capacitance               |  | -   | 8    | 30  | pF            |
| $C_{rss}$                      | reverse transfer capacitance     |  | -   | 4    | 10  | pF            |
| $t_{d(on)}$                    | turn-on delay time               | $V_{DS} = 50 \text{ V}; R_L = 250 \text{ } \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 50 \text{ } \Omega$   | -   | -    | -   | ns            |
| $t_r$                          | rise time                        |  | -   | -    | -   | ns            |
| $t_{d(off)}$                   | turn-off delay time              |  | -   | -    | -   | ns            |
| $t_f$                          | fall time                        |  | -   | -    | -   | ns            |
| $t_{off}$                      | turn-off time                    | $V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V}; R_{G(ext)} = 50 \text{ } \Omega; R_{GS} = 50 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}; R_L = 250 \text{ } \Omega$ | -   | 9    | -   | ns            |
| $t_{on}$                       | turn-on time                     |  | -   | 3    | -   | ns            |
| <b>Source-drain diode</b>      |                                  |  |     |      |     |               |
| $V_{SD}$                       | source-drain voltage             | $I_S = 300 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 13</a>  | -   | 0.93 | 1.5 | V             |
| $t_{rr}$                       | reverse recovery time            | $I_S = 300 \text{ mA}; di_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$                               | -   | 30   | -   | ns            |
| $Q_r$                          | recovered charge                 |  | -   | 30   | -   | nC            |



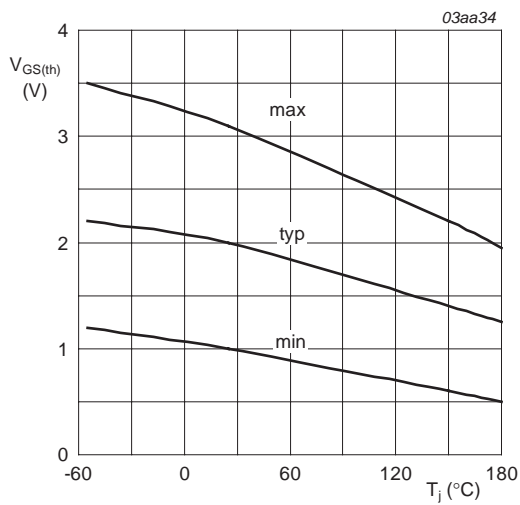
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



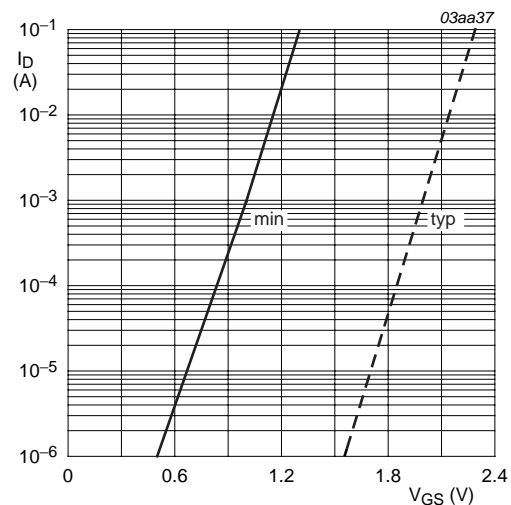
$V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



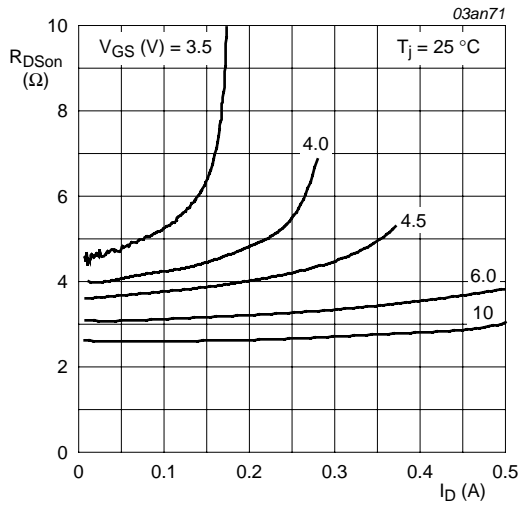
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 7. Gate-source threshold voltage as a function of junction temperature



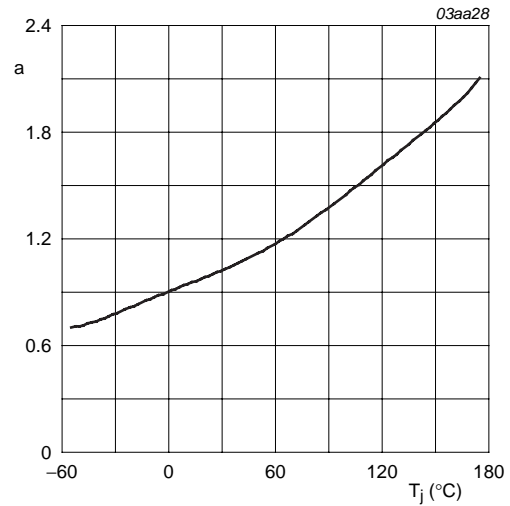
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 5\text{ V}$

Fig 8. Sub-threshold drain current as a function of gate-source voltage



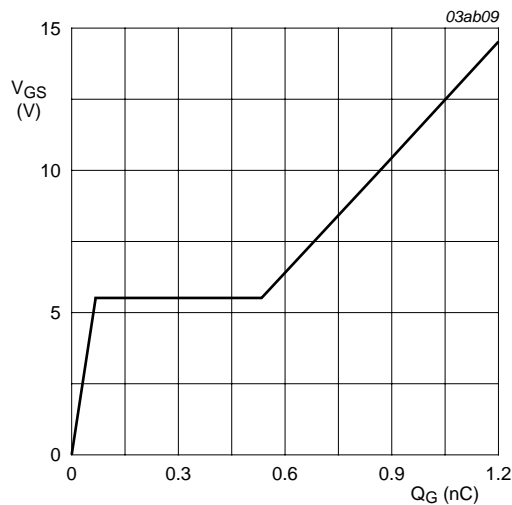
$T_j = 25^\circ C$

Fig 9. Drain-source on-state resistance as a function of drain current; typical values



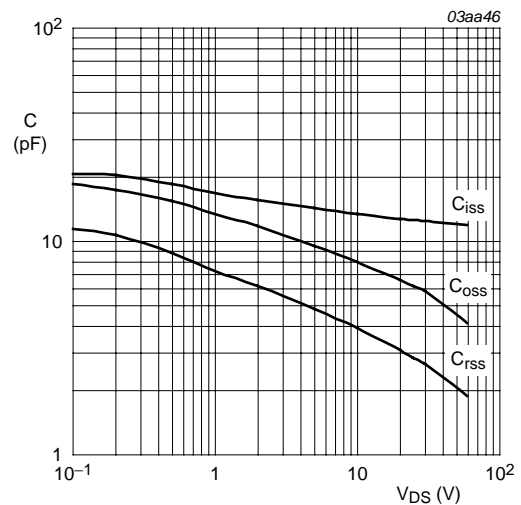
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



$I_D = 0.5 A; V_{DS} = 48 V$

Fig 11. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0 V; f = 1 MHz$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

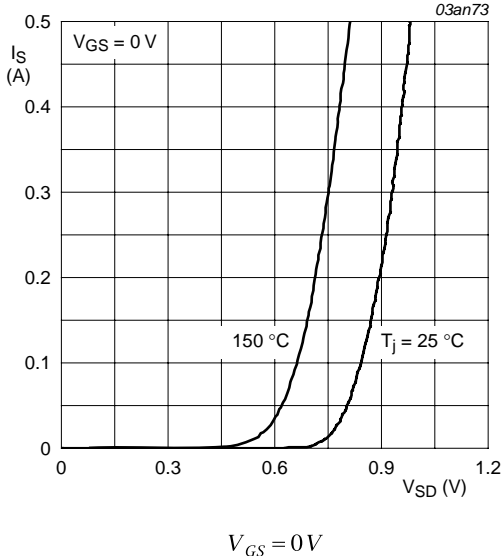


Fig 13. Source current as a function of source-drain voltage; typical values



8. Package outline

Plastic surface-mounted package; 3 leads

SOT323

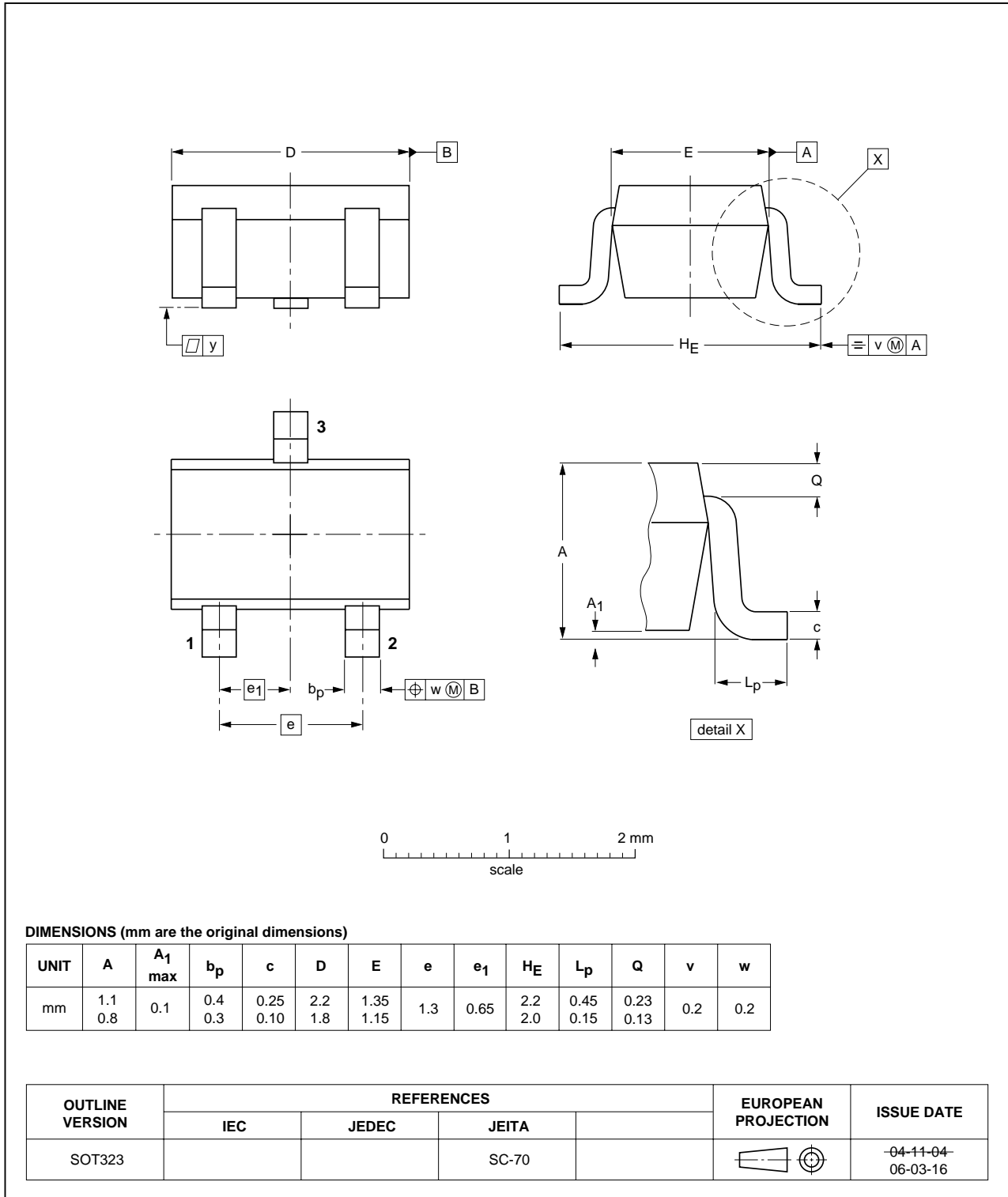


Fig 14. Package outline SOT323 (SC-70)

## 9. Revision history

**Table 8. Revision history**

| Document ID                  | Release date   | Data sheet status  | Change notice | Supersedes  |
|------------------------------|--|--------------------|---------------|-------------|
| PMF3800SN_3                  | 20091111   | Product data sheet | -             | PMF3800SN_2 |
| Modifications:               | <ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• Maximum value added for <math>V_{GS(th)}</math> @ <math>T_j = 25\text{ °C}</math> in Characteristics table.</li> </ul> |                    |               |             |
| PMF3800SN_2 (9397 750 15218) | 20050701   | Product data sheet | -             | PMF3800SN_1 |
| PMF3800SN_1 (9397 750 14255) | 20050208   | Product data sheet | -             | -           |

## 10. Legal information

### 10.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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