# PHKD6N02LT

## Dual N-channel TrenchMOS logic level FET

Rev. 04 — 27 April 2010 Product data sheet

## 1. Product profile

### 1.1 General description

Dual logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources

### 1.3 Applications

- Battery chargers
- DC-to-DC convertors
- Notebook computers
- Portable equipment

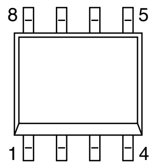
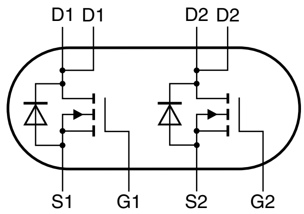
### 1.4 Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j \geq 25$ °C; $T_j \leq 150$ °C | - | - | 20 | V |
| $I_D$ | drain current | $T_{sp} = 25$ °C; Single device conducting; see Figure 1; see Figure 3 | - | - | 10.9 | A |
| $P_{tot}$ | total power dissipation | $T_{sp} = 25$ °C; see Figure 2 | - | - | 4.17 | W |
| **Static characteristics** | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS} = 2.5$ V; $I_D = 3$ A; $T_j = 25$ °C | - | 25 | 35 | mΩ |
| **Dynamic characteristics** | | | | | | |
| $Q_{GD}$ | gate-drain charge | $V_{GS} = 5$ V; $I_D = 6$ A; $V_{DS} = 16$ V; $T_j = 25$ °C; see Figure 11 | - | 6 | - | nC |

## 2. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | S1 | source1 |   SOT96-1 (SO8) |   mbk725 |
| 2 | G1 | gate1 | | |
| 3 | S2 | source2 | | |
| 4 | G2 | gate2 | | |
| 5 | D2 | drain2 | | |
| 6 | D2 | drain2 | | |
| 7 | D1 | drain1 | | |
| 8 | D1 | drain1 | | |

## 3. Ordering information

**Table 3. Ordering information**

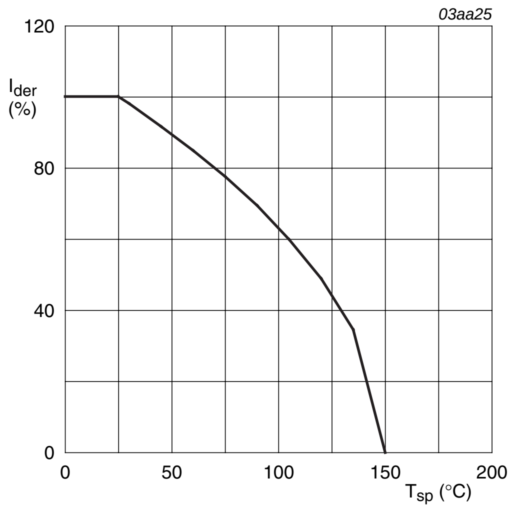
| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PHKD6N02LT | SO8 | plastic small outline package; 8 leads; body width 3.9 mm | SOT96-1 |

## 4. Limiting values

**Table 4. Limiting values**

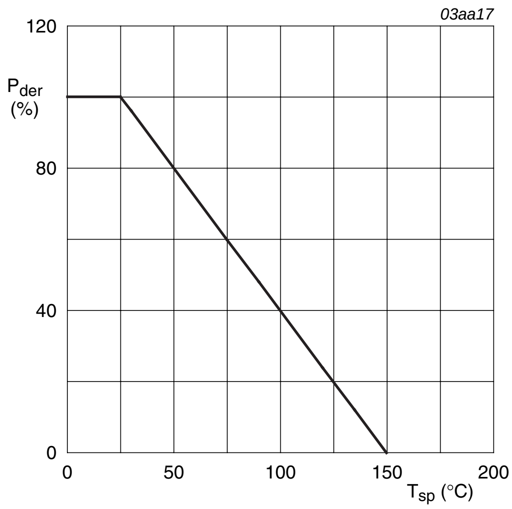
*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j \geq 25$ °C; $T_j \leq 150$ °C | - | - | 20 | V |
| $V_{DGR}$ | drain-gate voltage | $T_j \leq 150$ °C; $T_j \geq 25$ °C; $R_{GS} = 20$ kΩ | - | - | 20 | V |
| $V_{GS}$ | gate-source voltage | | -12 | - | 12 | V |
| $I_D$ | drain current | $T_{sp} = 100$ °C; Single device conducting; see Figure 1 | - | - | 6.8 | A |
| | | $T_{sp} = 25$ °C; Single device conducting; see Figure 1; see Figure 3 | - | - | 10.9 | A |
| $I_{DM}$ | peak drain current | $T_{sp} = 25$ °C; $t_p \leq 100$ µs; pulsed; Single device conducting; see Figure 3 | - | - | 44 | A |
| $P_{tot}$ | total power dissipation | $T_{sp} = 25$ °C; see Figure 2 | - | - | 4.17 | W |
| $T_{stg}$ | storage temperature | | -55 | - | 150 | °C |
| $T_j$ | junction temperature | | -55 | - | 150 | °C |
| **Source-drain diode** | | | | | | |
| $I_S$ | source current | $T_{sp} = 25$ °C | - | - | 3.5 | A |
| $I_{SM}$ | peak source current | $T_{sp} = 25$ °C; $t_p \leq 10$ µs; pulsed | - | - | 44 | A |



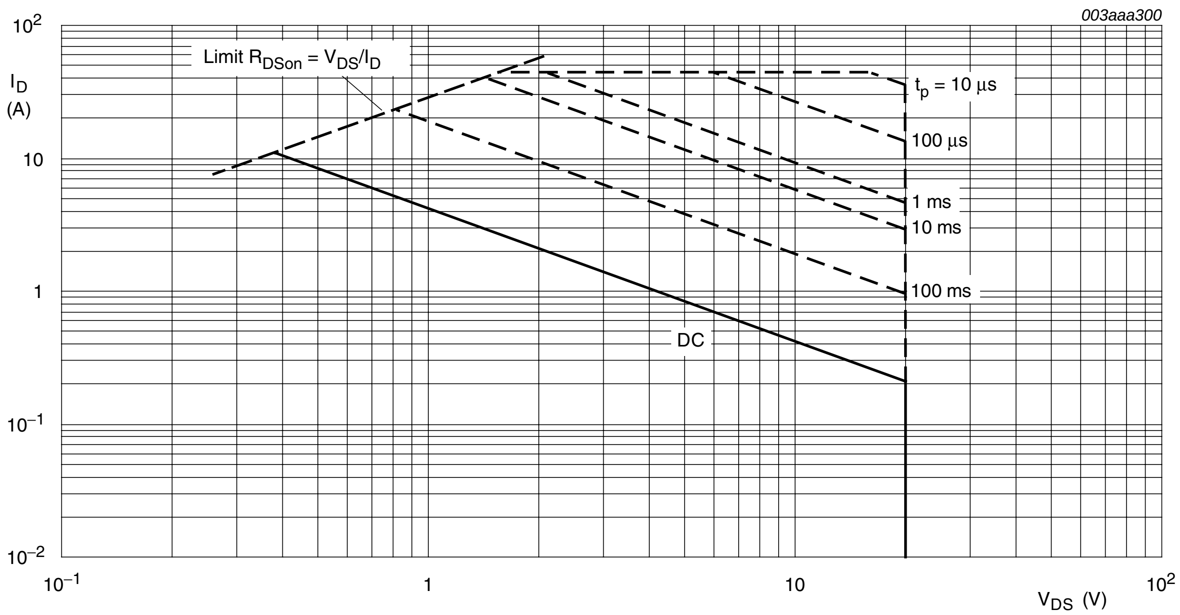

$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

**Fig 1. Normalized continuous drain current as a function of solder point temperature**




$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

**Fig 2. Normalized total power dissipation as a function of solder point temperature**




$T_{sp} = 25°C; I_{DM}$ is single pulse;

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | see Figure 4 | - | - | 30 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | minimum footprint; mounted on printed-circuit board | - | 70 | - | K/W |

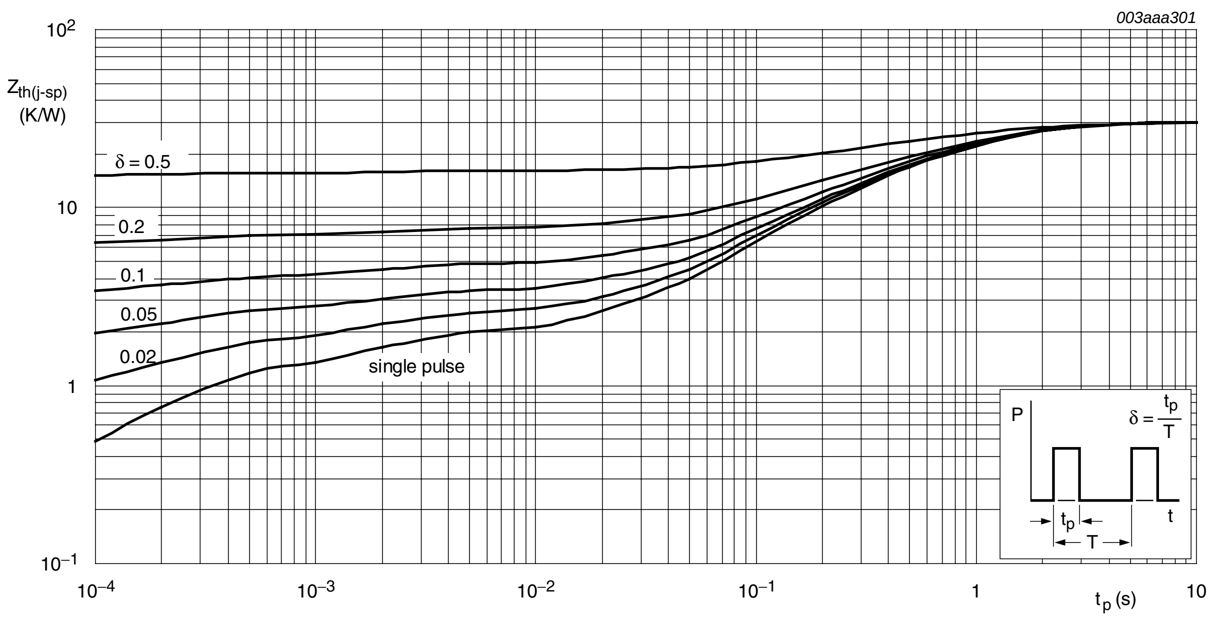
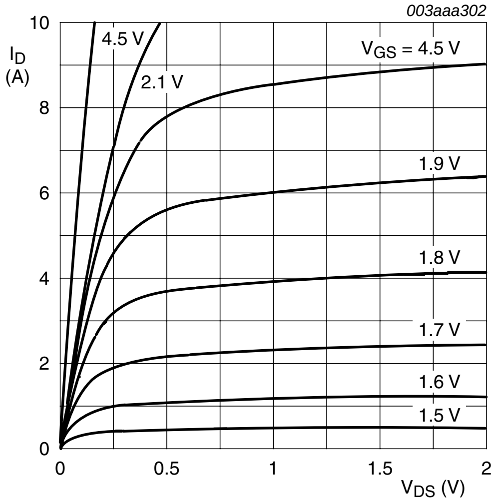



**Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration**

# 6. Characteristics

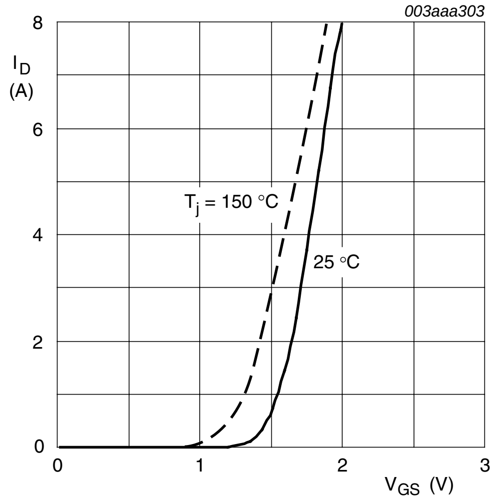
Table 6. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | 20 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 250 µA; $V_{DS}$ = 10 V; $T_j$ = 25 °C; see Figure 8 | 0.5 | - | 1.5 | V |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 20 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | - | 0.05 | 10 | µA |
| | | $V_{DS}$ = 20 V; $V_{GS}$ = 0 V; $T_j$ = 150 °C | - | - | 500 | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 12 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | - | - | 100 | nA |
| | | $V_{GS}$ = -12 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | - | - | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 2.5 V; $I_D$ = 3 A; $T_j$ = 25 °C | - | 25 | 35 | mΩ |
| | | $V_{GS}$ = 5 V; $I_D$ = 3 A; $T_j$ = 150 °C; see Figure 9; see Figure 10 | - | - | 35 | mΩ |
| | | $V_{GS}$ = 5 V; $I_D$ = 3 A; $T_j$ = 25 °C; see Figure 9; see Figure 10 | - | 16 | 20 | mΩ |
| **Dynamic characteristics** | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 6 A; $V_{DS}$ = 16 V; $V_{GS}$ = 5 V; $T_j$ = 25 °C; see Figure 11 | - | 15.3 | - | nC |
| $Q_{GS}$ | gate-source charge | | - | 2.2 | - | nC |
| $Q_{GD}$ | gate-drain charge | | - | 6 | - | nC |
| $C_{iss}$ | input capacitance | $V_{DS}$ = 10 V; $V_{GS}$ = 0 V; f = 1 MHz; $T_j$ = 25 °C; see Figure 12 | - | 950 | - | pF |
| $C_{oss}$ | output capacitance | | - | 355 | - | pF |
| $C_{rss}$ | reverse transfer capacitance | | - | 256 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 10 V; $R_L$ = 3.3 Ω; $V_{GS}$ = 5 V; $R_{G(ext)}$ = 4.7 Ω; $T_j$ = 25 °C | - | 15 | - | ns |
| $t_r$ | rise time | | - | 49 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 50 | - | ns |
| $t_f$ | fall time | | - | 23 | - | ns |
| **Source-drain diode** | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 6 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C; see Figure 13 | - | - | 1.2 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 6 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 20 V; $T_j$ = 25 °C | - | 40 | - | ns |
| $Q_r$ | recovered charge | | - | 7 | - | nC |



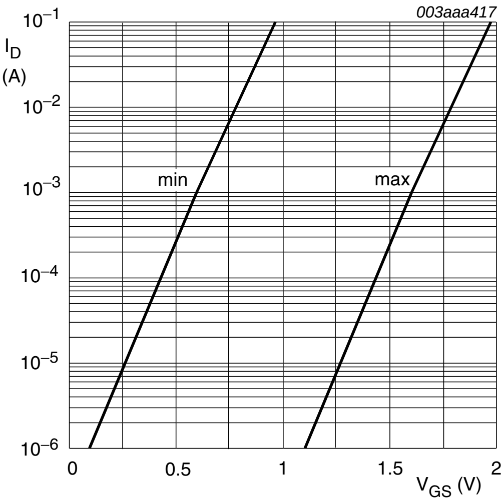

$T_j = 25°C$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



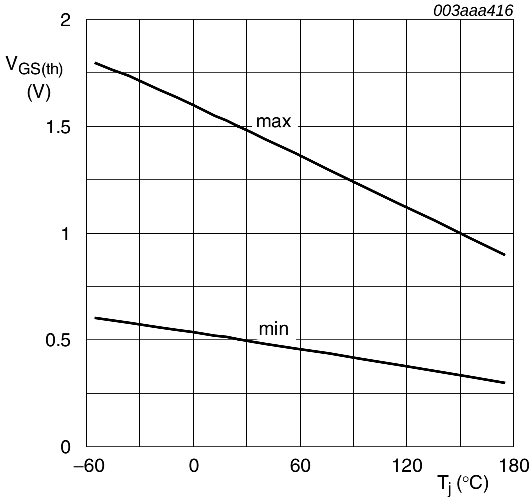

$T_j = 25°C$ and $150°C; V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



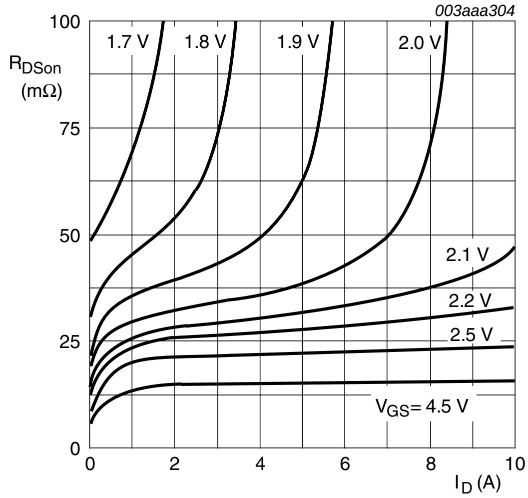

$T_j = 25°C; V_{DS} = 5V$

Fig 7. Sub-threshold drain current as a function of gate-source voltage



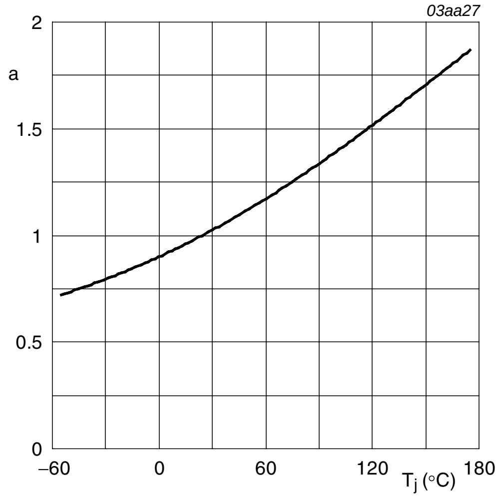

$I_D = 1mA; V_{DS} = V_{GS}$

Fig 8. Gate-source threshold voltage as a function of junction temperature



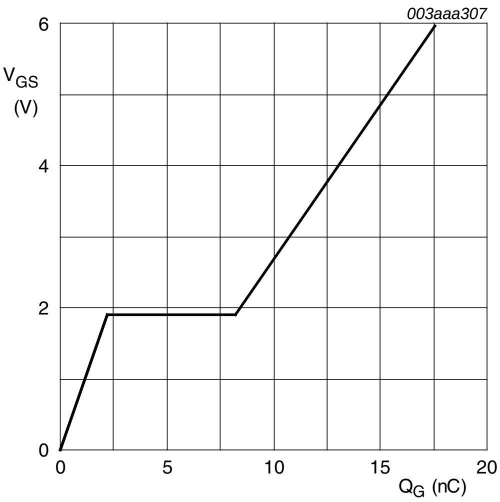

$T_j = 25°C$

Fig 9. Drain-source on-state resistance as a function of drain current; typical values



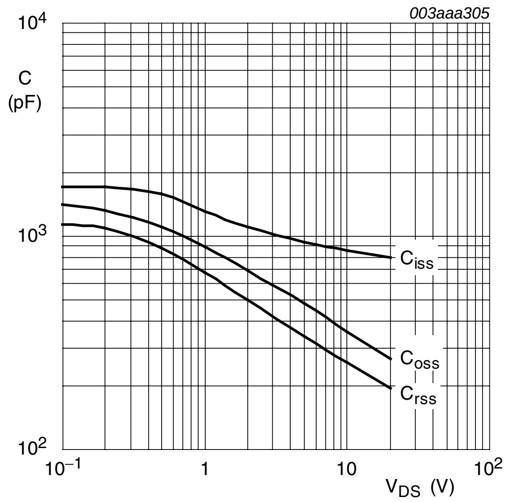

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



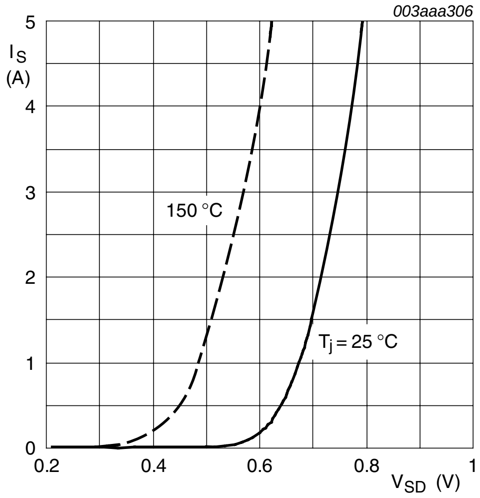

$I_D = 6A; V_{DD} = 16V$

Fig 11. Gate-source voltage as a function of gate charge; typical values




$V_{GS} = 0V; f = 1MHz$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical val

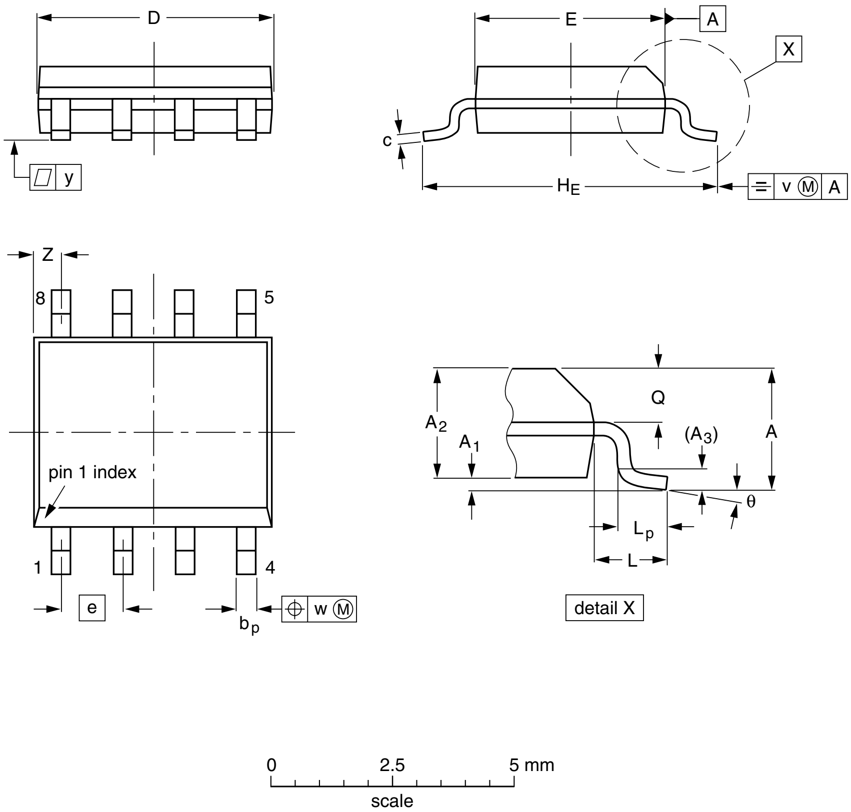



$T_j = 25°C$ and $150°C; V_{GS} = 0V$

**Fig 13. Source current as a function of source-drain voltage; typical values**

# 7. Package outline

**SO8: plastic small outline package; 8 leads; body width 3.9 mm** **SOT96-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D(1) | E(2) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z(1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 5.0<br>4.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | 8°<br>0° |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.20<br>0.19 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.024 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Notes**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

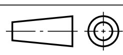
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT96-1 | 076E03 | MS-012 | | |  | ~~99-12-27~~<br>03-02-18 |

**Fig 14. Package outline SOT96-1 (SO8)**

## 8. Revision history

Table 7. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PHKD6N02LT_4 | 20100427 | Product data sheet | - | PHKD6N02LT_3 |
| Modifications: | • Various changes to content. | | | |
| PHKD6N02LT_3 | 20091119 | Product data sheet | - | PHKD6N02LT-02 |
| PHKD6N02LT-02 | 20030812 | Product data | - | PHKD6N02LT-01 |
| PHKD6N02LT-01 | 20010907 | Product data | - | - |

# 9. Legal information

## 9.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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For sales office addresses, please send an email to: salesaddresses@nxp.com

## 11. Contents





**Date of release: 27 April 2010**

**Document identifier: PHKD6N02LT**