

# PH1875L

## N-channel TrenchMOS logic level FET

Rev. 01 — 29 November 2005

Product data sheet

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

### 1.2 Features

- Logic level threshold
- Low thermal resistance
- Very low on-state resistance
- Surface-mounted package

### 1.3 Applications

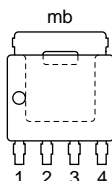
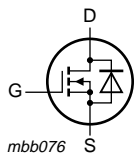
- DC motor control
- DC-to-DC converters
- General purpose power switching

### 1.4 Quick reference data

- $V_{DS} \leq 75 \text{ V}$
- $R_{DS(on)} \leq 16.5 \text{ m}\Omega$
- $I_D \leq 45.8 \text{ A}$
- $Q_{GD} = 15.3 \text{ nC (typ)}$

## 2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 3	source (S)		
4	gate (G)		
mb	mounting base; connected to drain (D)		

**SOT669 (LFPACK)**

# PHILIPS

### 3. Ordering information

**Table 2: Ordering information**

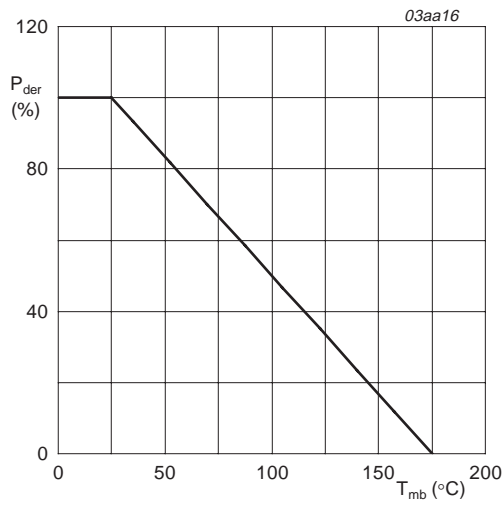
Type number	Package		Version
	Name	Description	
PH1875L	LFAK	plastic single-ended surface mounted package; 4 leads	SOT669

### 4. Limiting values

**Table 3: Limiting values**

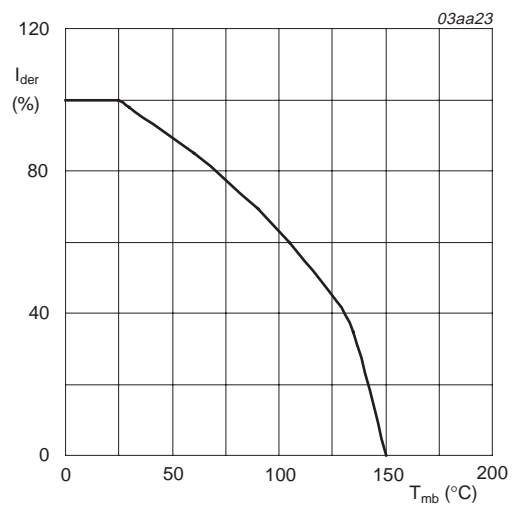
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	75	V
$V_{DGR}$	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	75	V
$V_{GS}$	gate-source voltage		-	$\pm 15$	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 2</a> and <a href="#">3</a>	-	45.8	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 2</a>	-	29	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; see <a href="#">Figure 3</a>	-	183	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>	-	62.5	W
$T_{stg}$	storage temperature		-55	+150	$^{\circ}\text{C}$
$T_j$	junction temperature		-55	+150	$^{\circ}\text{C}$
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	45.8	A
$I_{SM}$	peak source current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	183	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 26\text{ A}$ ; $t_p = 0.11\text{ ms}$ ; $V_{DS} \leq 75\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; starting at $T_j = 25\text{ °C}$	-	165	mJ



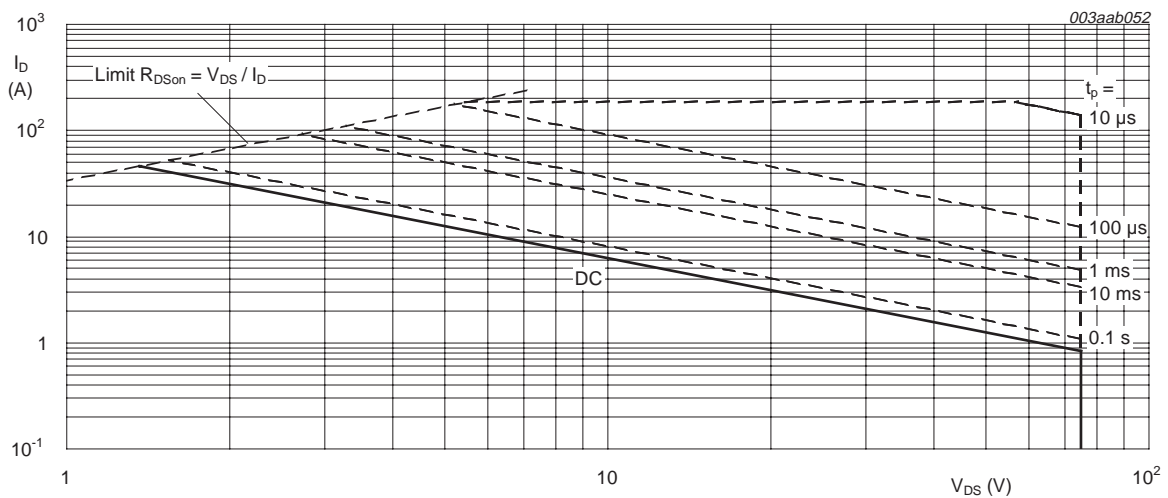
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



T<sub>mb</sub> = 25 °C; I<sub>DM</sub> is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## 5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	2	K/W

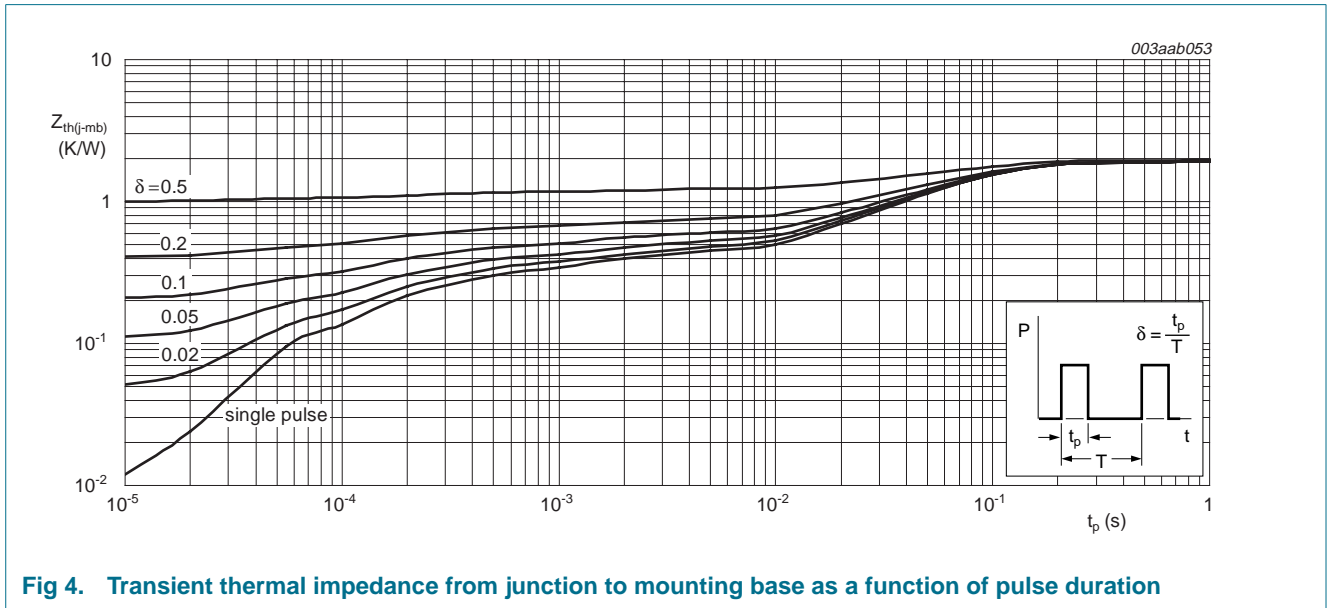
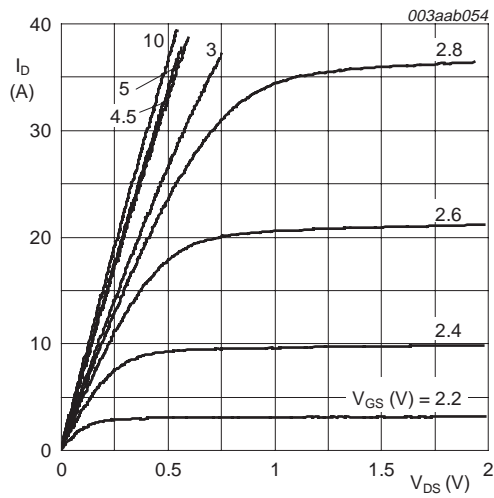


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

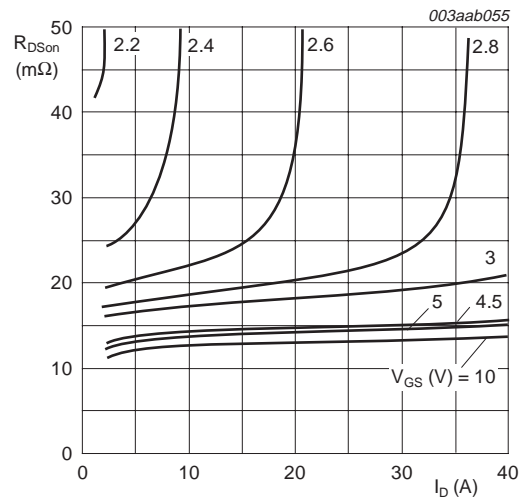
**Table 5: Characteristics**
 $T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$ ; $V_{GS} = 0\text{ V}$ $T_j = 25\text{ }^\circ\text{C}$	75	-	-	V
		$T_j = -55\text{ }^\circ\text{C}$	68	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$ ; $V_{DS} = V_{GS}$ ; see <a href="#">Figure 9</a> and <a href="#">10</a> $T_j = 25\text{ }^\circ\text{C}$	1	1.5	2	V
		$T_j = 150\text{ }^\circ\text{C}$	0.5	-	-	V
		$T_j = -55\text{ }^\circ\text{C}$	-	-	2.2	V
$I_{DSS}$	drain leakage current	$V_{DS} = 75\text{ V}$ ; $V_{GS} = 0\text{ V}$ $T_j = 25\text{ }^\circ\text{C}$	-	-	1	$\mu\text{A}$
		$T_j = 150\text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = \pm 15\text{ V}$ ; $V_{DS} = 0\text{ V}$	-	10	100	nA
$R_G$	gate resistance	$f = 1\text{ MHz}$	-	1	-	$\Omega$
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 20\text{ A}$ ; see <a href="#">Figure 6</a> and <a href="#">8</a> $T_j = 25\text{ }^\circ\text{C}$	-	13.3	16.5	m $\Omega$
		$T_j = 150\text{ }^\circ\text{C}$	-	24.2	30	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ ; $I_D = 20\text{ A}$ ; see <a href="#">Figure 6</a> and <a href="#">8</a>	-	14.6	20	m $\Omega$
		$V_{GS} = 5\text{ V}$ ; $I_D = 20\text{ A}$ ; see <a href="#">Figure 6</a> and <a href="#">8</a>	-	14.2	18	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25\text{ A}$ ; $V_{DS} = 60\text{ V}$ ; $V_{GS} = 5\text{ V}$ ; see <a href="#">Figure 11</a> and <a href="#">12</a>	-	33.4	-	nC
$Q_{GS}$	gate-source charge		-	6.7	-	nC
$Q_{GS1}$	pre- $V_{GS(th)}$ gate-source charge		-	3.3	-	nC
$Q_{GS2}$	post- $V_{GS(th)}$ gate-source charge		-	3.4	-	nC
$Q_{GD}$	gate-drain charge		-	15.3	-	nC
$V_{GS(pl)}$	gate-source plateau voltage		-	3	-	V
$Q_{G(tot)}$	total gate charge	$I_D = 0\text{ A}$ ; $V_{DS} = 0\text{ V}$ ; $V_{GS} = 4.5\text{ V}$	-	23	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 25\text{ V}$ ; $f = 1\text{ MHz}$ ; see <a href="#">Figure 14</a>	-	2600	-	pF
$C_{oss}$	output capacitance		-	285	-	pF
$C_{rss}$	reverse transfer capacitance		-	150	-	pF
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 0\text{ V}$ ; $f = 1\text{ MHz}$	-	4000	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}$ ; $R_L = 1.2\text{ }\Omega$ ; $V_{GS} = 5\text{ V}$ ; $R_G = 10\text{ }\Omega$	-	23	-	ns
$t_r$	rise time		-	80	-	ns
$t_{d(off)}$	turn-off delay time		-	92	-	ns
$t_f$	fall time		-	60	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; see <a href="#">Figure 13</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}$ ; $dI_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ;	-	107	-	ns
$Q_r$	recovered charge	$V_R = 30\text{ V}$	-	124	-	nC



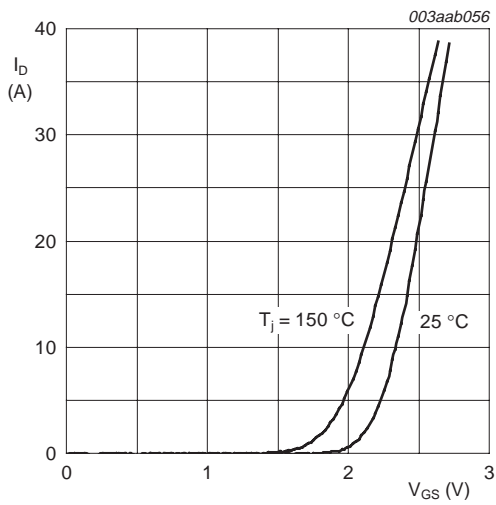
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



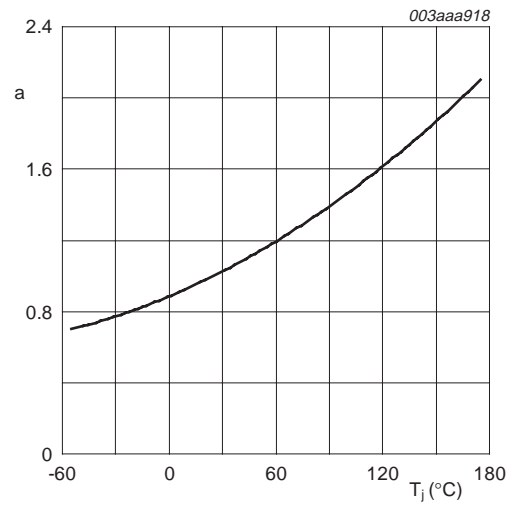
$T_j = 25^\circ\text{C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



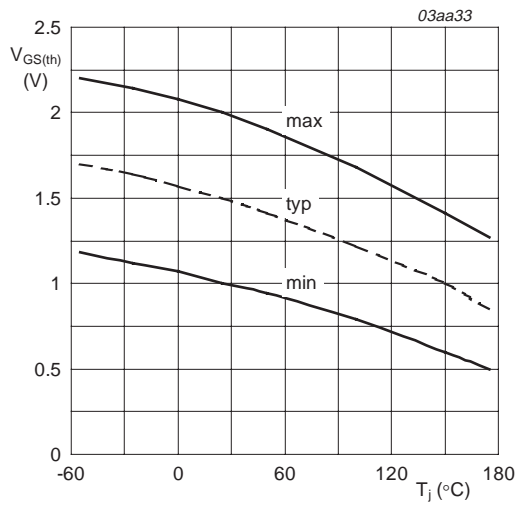
$T_j = 25^\circ\text{C}$  and  $150^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



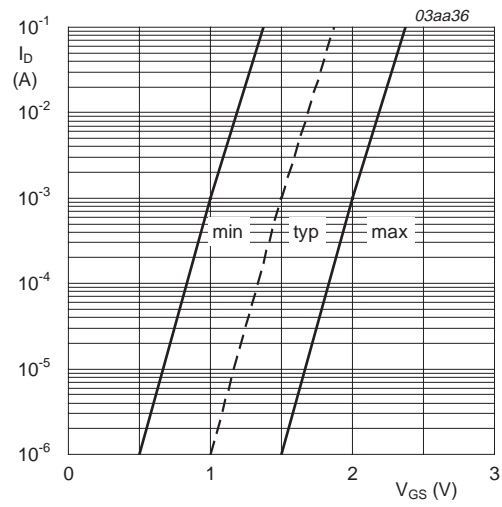
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



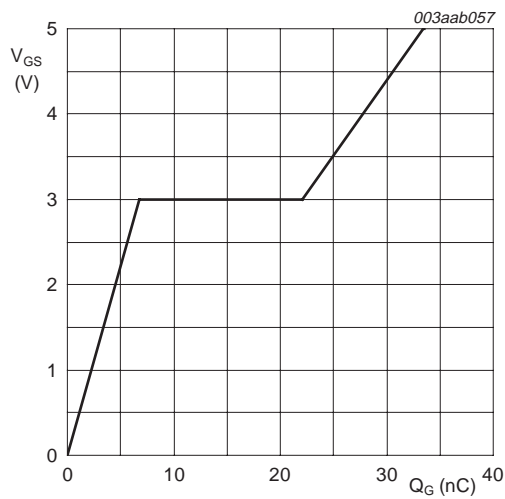
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$I_D = 25 \text{ A}; V_{DS} = 60 \text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values

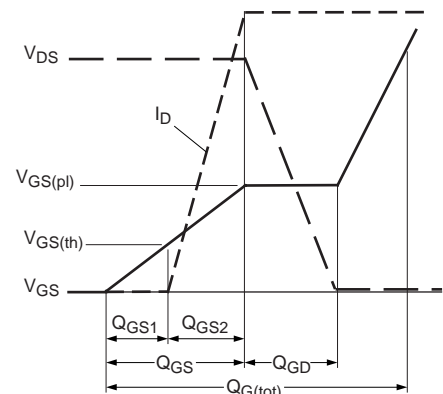
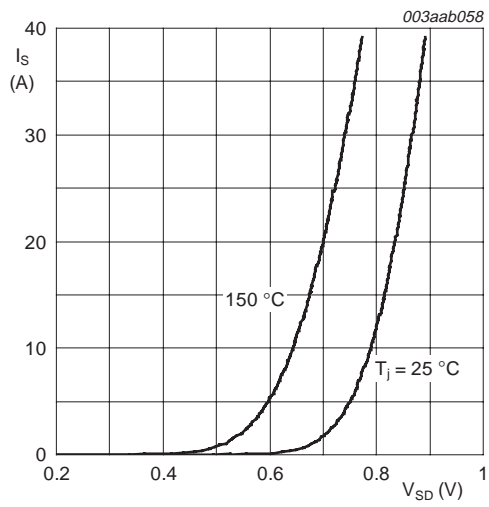
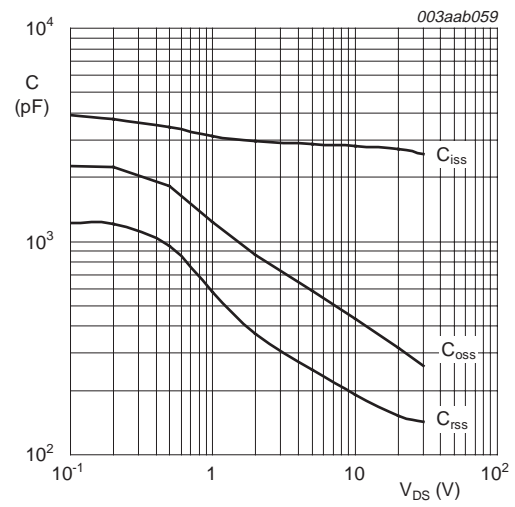


Fig 12. Gate charge waveform definitions



$T_j = 25^\circ\text{C}$  and  $150^\circ\text{C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 13. Source current as a function of source-drain voltage; typical values**



$V_{GS} = 0\text{ V}$ ;  $f = 1\text{ MHz}$

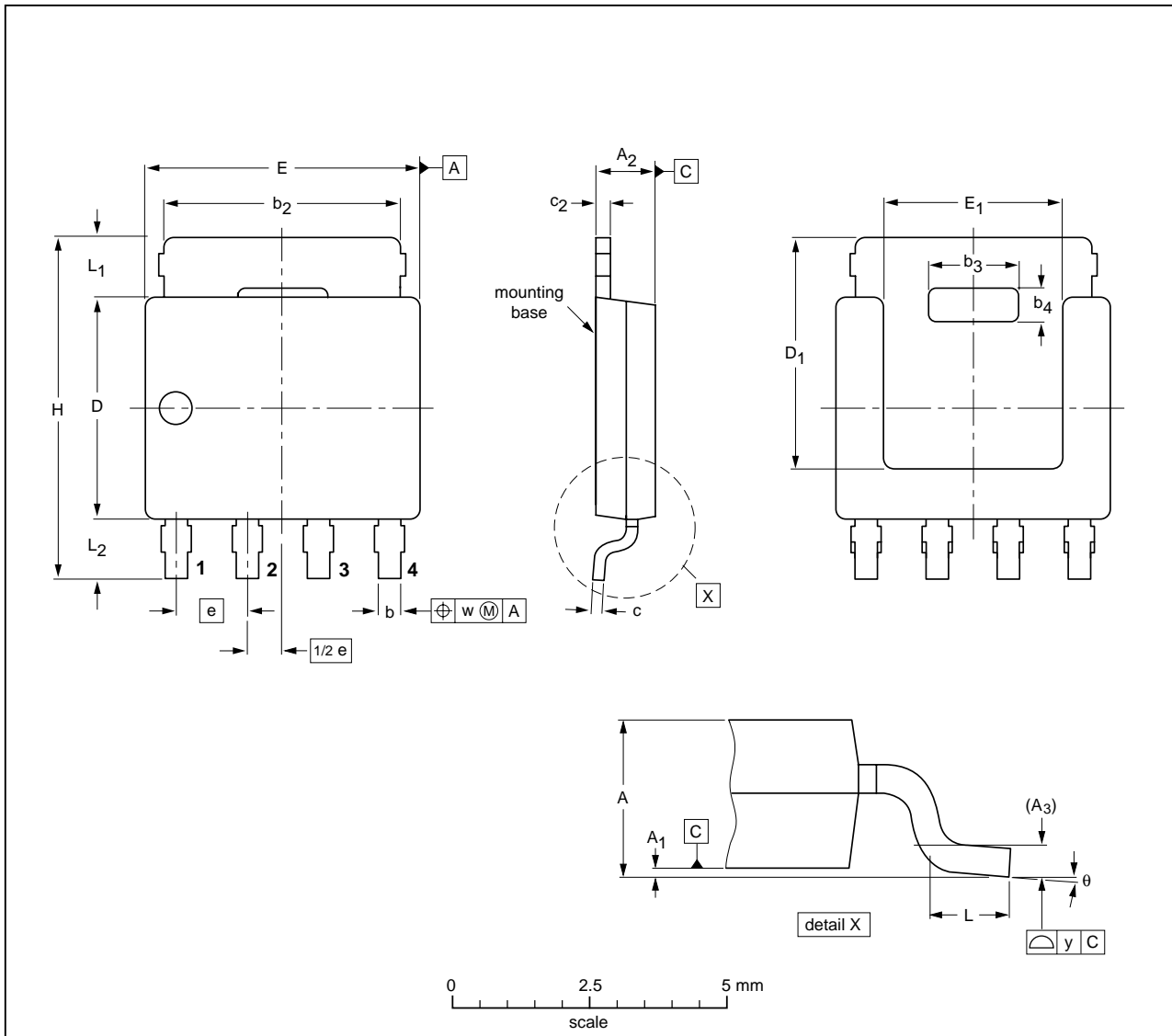
**Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



7. Package outline

Plastic single-ended surface mounted package (LPAK); 4 leads

SOT669



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>	c	c <sub>2</sub>	D <sup>(1)</sup>	D <sub>1</sub> <sup>(1)</sup> max	E <sup>(1)</sup>	E <sub>1</sub> <sup>(1)</sup>	e	H	L	L <sub>1</sub>	L <sub>2</sub>	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT669		MO-235				03-09-15 04-10-13

Fig 15. Package outline SOT669 (LPAK)

## 8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PH1875L_1	20051129	Product data sheet	-	-	-

## 9. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2] [3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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