



BUK9Y3R5-40E

N-channel 40 V, 3.8 mΩ logic level MOSFET in LFAK56

11 November 2014

Product data sheet

1. General description

Logic level N-channel MOSFET in an LFAK56 (Power SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Q101 Compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with $V_{GS(th)}$ rating of greater than 0.5 V at 175 °C

3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	40	V
I_D	drain current	$V_{GS} = 5\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 2}$	[1]	-	100	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	167	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}; \text{Fig. 11}$	-	2.9	3.8	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 5\text{ V}; I_D = 25\text{ A}; V_{DS} = 32\text{ V}; T_j = 25\text{ °C}; \text{Fig. 13}; \text{Fig. 14}$	-	8.6	-	nC

[1] Continuous current is limited by package.

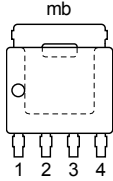
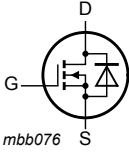


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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK56; Power-SO8 (SOT669)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK9Y3R5-40E	LPAK56; Power-SO8	Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9Y3R5-40E	93E540

8. Limiting values

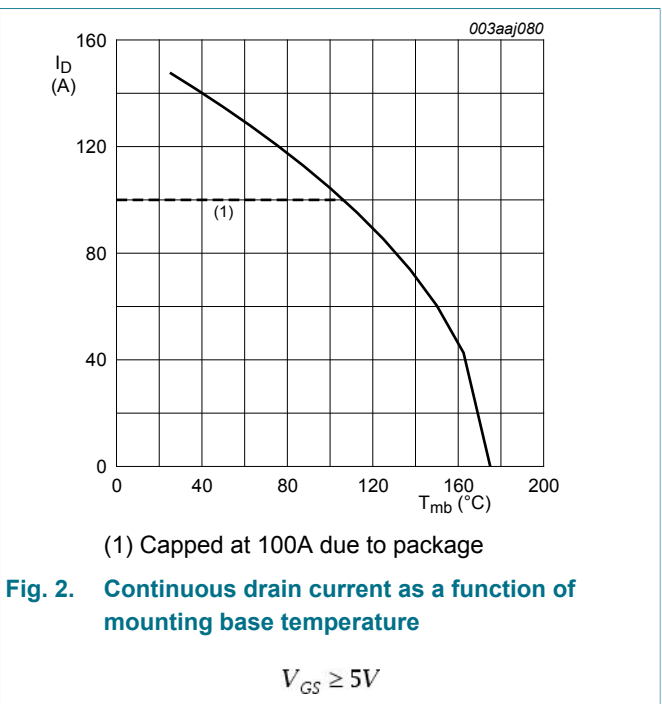
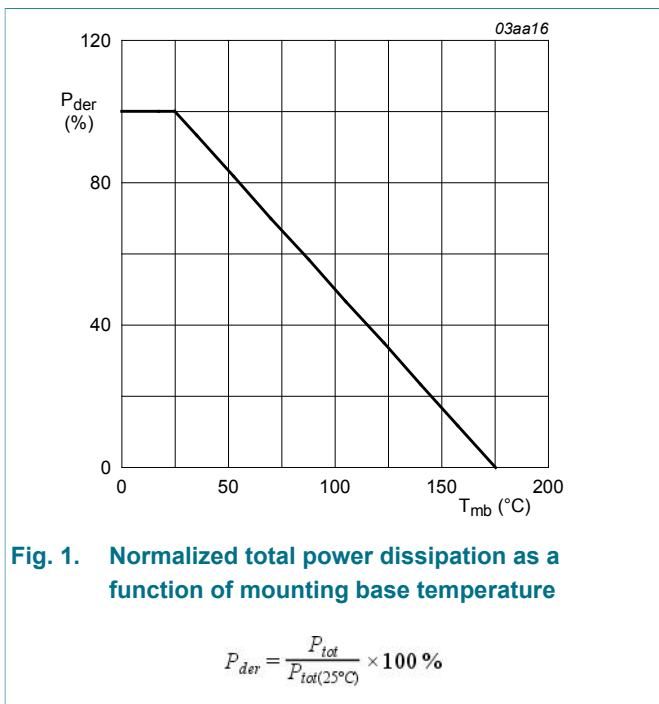
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	40	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	40	V
V_{GS}	gate-source voltage	$T_j \leq 175\text{ °C}$; DC	-10	10	V
		$T_j \leq 175\text{ °C}$; Pulsed	[1][2]	15	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	167	W
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 5\text{ V}$; Fig. 2	[3]	100	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 5\text{ V}$; Fig. 2	[3]	100	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Fig. 3	-	591	A

Symbol	Parameter	Conditions		Min	Max	Unit
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C	[3]	-	100	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	591	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 100 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 5 V; T _{j(init)} = 25 °C; unclamped; Fig. 4	[4][5]	-	135	mJ

- [1] Accumulated pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T_j and or V_{GS}
- [3] Continuous current is limited by package.
- [4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [5] Refer to application note AN10273 for further information.



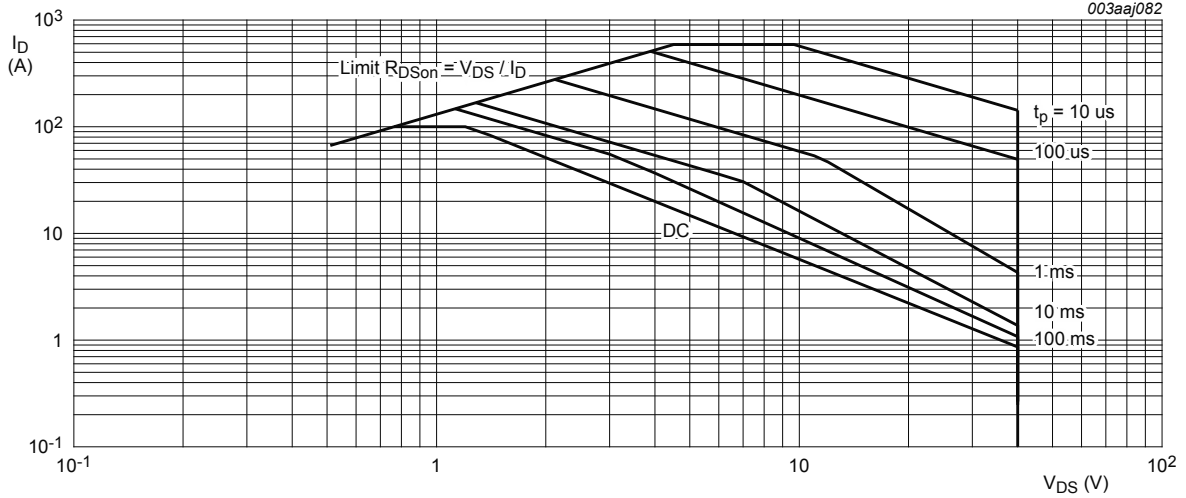


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^\circ C$; I_{DM} is a single pulse

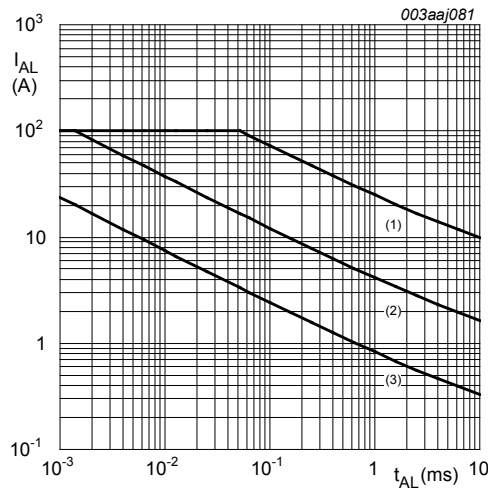


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j(jmt)} = 25^\circ C$; (2) $T_{j(jmt)} = 150^\circ C$; (3) Repetitive Avalanche

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	0.9	K/W

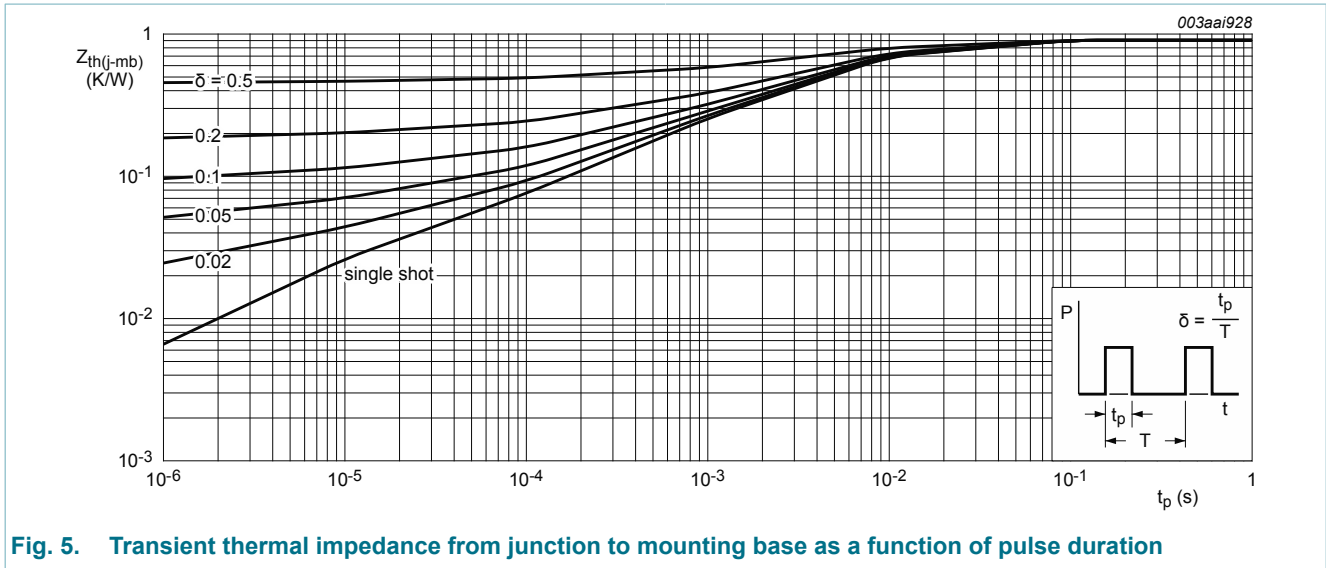


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

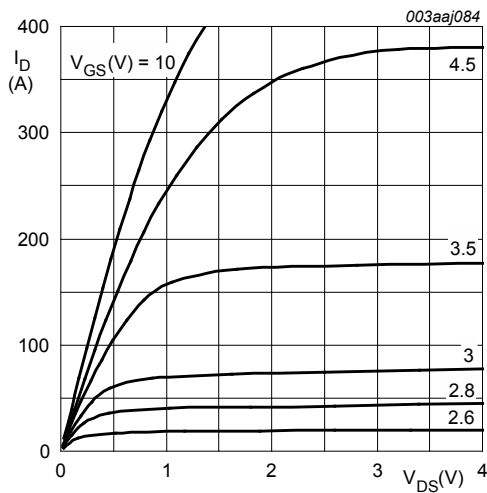
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ Fig. 9; Fig. 10	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ Fig. 9	-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ Fig. 9	0.5	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.07	10	μA
		$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5 V; I_D = 25 A; T_j = 25 \text{ }^\circ C;$ Fig. 11	-	2.9	3.8	mΩ
		$V_{GS} = 10 V; I_D = 25 A; T_j = 25 \text{ }^\circ C;$ Fig. 11	-	2.3	3.6	mΩ
		$V_{GS} = 5 V; I_D = 25 A; T_j = 175 \text{ }^\circ C;$ Fig. 11; Fig. 12	-	-	7.6	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 A; V_{DS} = 32 V; V_{GS} = 5 V;$ $T_j = 25 \text{ }^\circ C;$ Fig. 13; Fig. 14	-	30.2	-	nC
Q_{GS}	gate-source charge		-	9.7	-	nC

N-channel 40 V, 3.8 mΩ logic level MOSFET in LPAK56

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Q_{GD}	gate-drain charge		-	8.6	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C};$ Fig. 15	-	3852	5137	pF
C_{oss}	output capacitance		-	487	584	pF
C_{rss}	reverse transfer capacitance		-	222	304	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}; R_L = 1.2\text{ }\Omega; V_{GS} = 5\text{ V}; R_{G(ext)} = 5\text{ }\Omega; T_j = 25\text{ }^\circ\text{C}$	-	20.2	-	ns
t_r	rise time		-	36.8	-	ns
$t_{d(off)}$	turn-off delay time		-	43.2	-	ns
t_f	fall time		-	29.5	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 16	-	0.82	1.2	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	26	-	ns
Q_r	recovered charge		-	19.4	-	nC



$T_j = 25\text{ }^\circ\text{C}; t_p = 300\text{ }\mu\text{s}$

Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

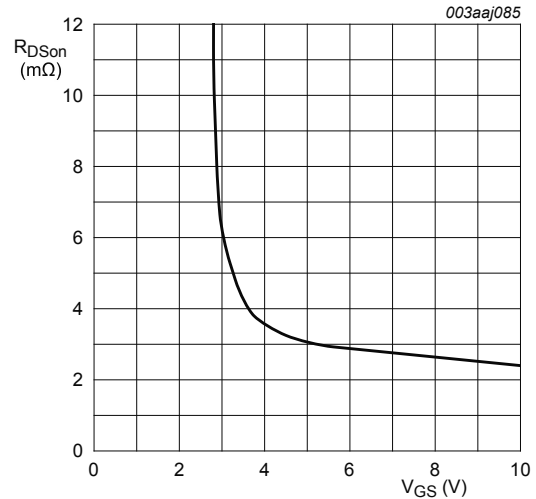


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$

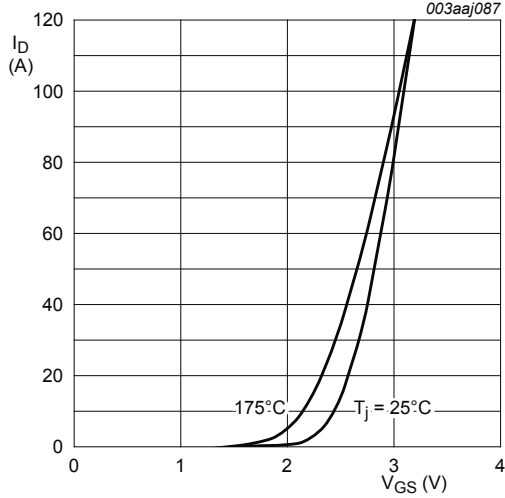


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10V$



Fig. 9. Gate-source threshold voltage as a function of junction temperature

$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

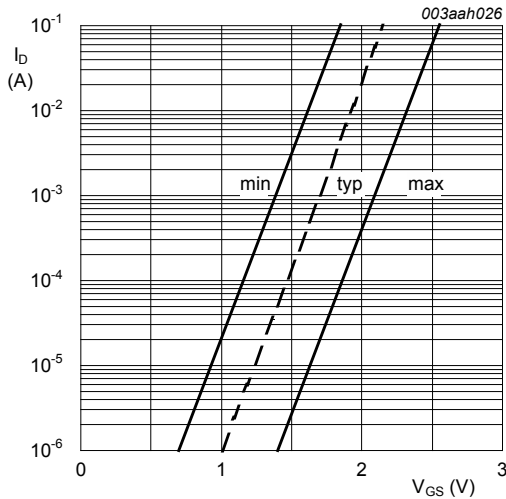
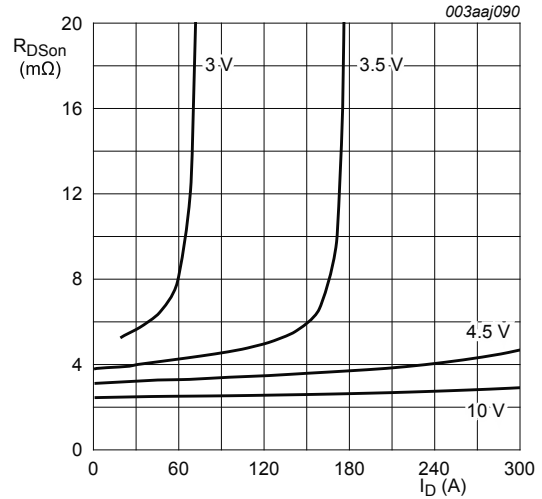


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ\text{C}; V_{DS} = 5V$



$T_j = 25^\circ\text{C}; t_p = 300 \mu\text{s}$

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

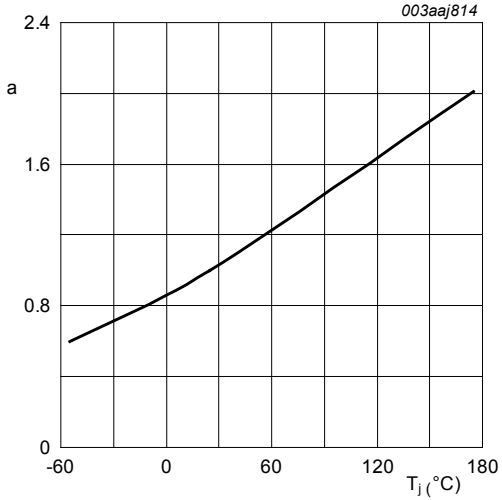


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)}(25^\circ\text{C})}$$

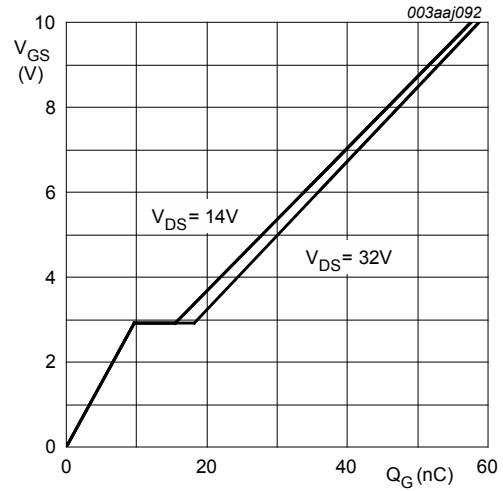


Fig. 13. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^\circ\text{C}; I_D = 25\text{A}$$

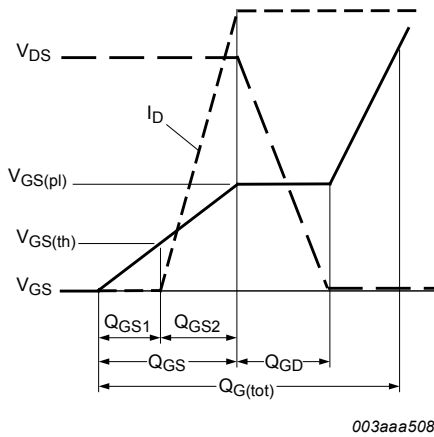


Fig. 14. Gate charge waveform definitions

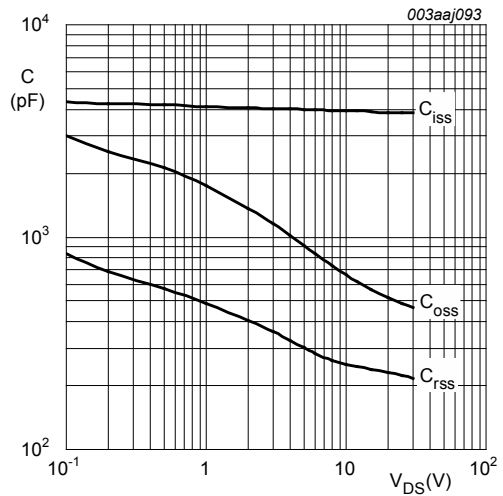
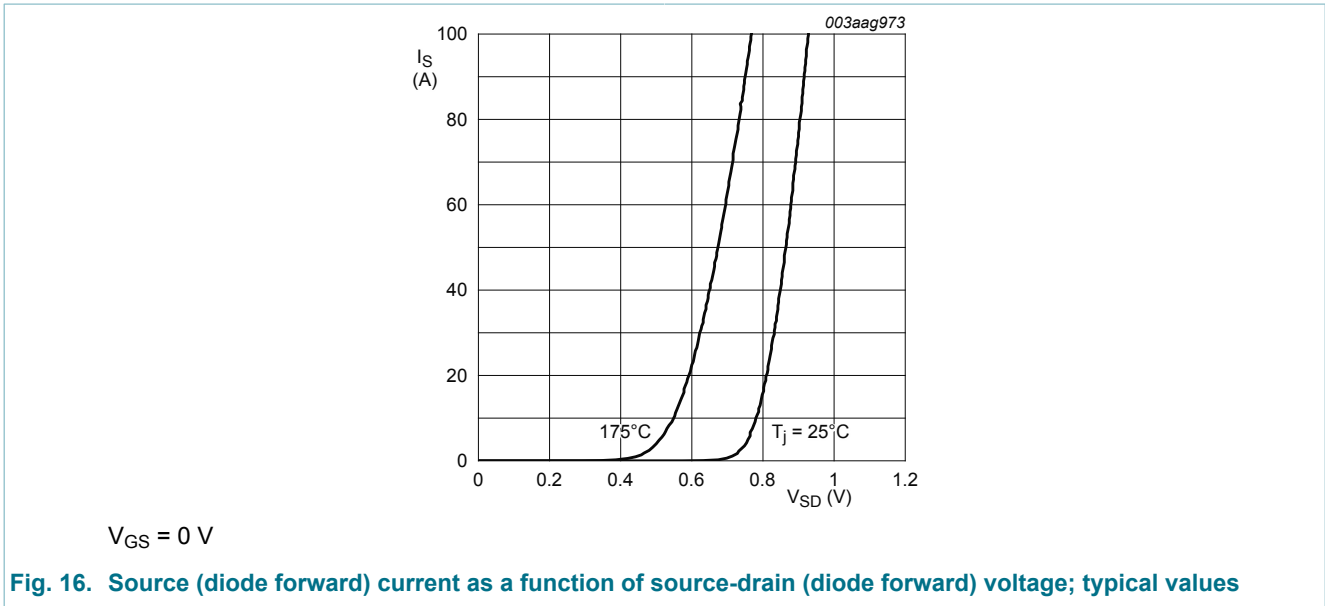


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0\text{V}; f = 1\text{MHz}$$



11. Package outline

Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads SOT669



Dimensions (mm are the original dimensions)

Unit ⁽¹⁾	A	A ₁	A ₂	A ₃	b	b ₂	b ₃	b ₄	c	c ₂	D ⁽¹⁾	D ₁ ⁽¹⁾	E ⁽¹⁾	E ₁ ⁽¹⁾	e	H	L	L ₁	L ₂	w	y
max	1.20	0.15	1.10		0.50	4.41	2.2	0.9	0.25	0.30	4.10	4.20	5.0	3.3		6.2	0.85	1.3	1.3		
nom				0.25											1.27					0.25	0.1
min	1.01	0.00	0.95		0.35	3.62	2.0	0.7	0.19	0.24	3.80		4.8	3.1		5.8	0.40	0.8	0.8		

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

sot669_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT669		MO-235				-11-03-25- 13-02-27

Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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