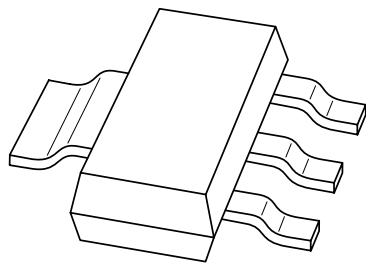


# DATA SHEET



## **BSP130**

**N-channel enhancement mode  
vertical D-MOS transistor**

Product specification  
Supersedes data of 1997 Jun 23

2001 Dec 11

# N-channel enhancement mode vertical D-MOS transistor

## BSP130

### FEATURES

- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

### APPLICATIONS

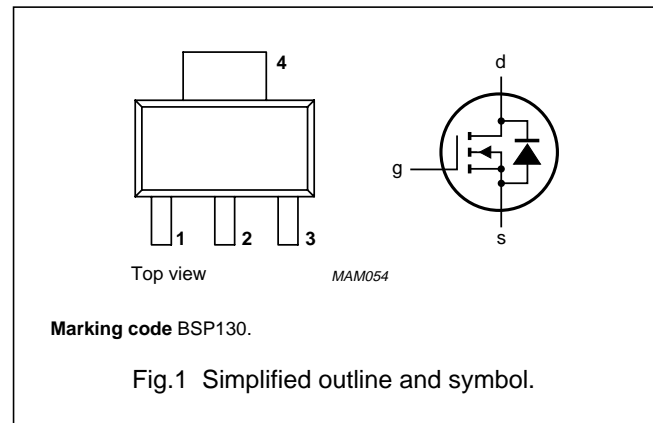
- Line current interruptor in telephone sets
- Relay, high-speed and line transformer drivers.

### DESCRIPTION

N-channel enhancement mode vertical D-MOS transistor in a SOT223 package.

### PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain



### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage (DC)		–	300	V
$I_D$	drain current (DC)		–	350	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$	–	1.5	W
$V_{GSO}$	gate-source voltage	open drain	–	$\pm 20$	V
$R_{DSon}$	drain-source on-state resistance	$I_D = 250\text{ mA}; V_{GS} = 10\text{ V}$	–	6	$\Omega$
$V_{GSoff}$	gate-source cut-off voltage	$I_D = 1\text{ mA}; V_{DS} = V_{GS}$	0.8	2	V

### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	drain-source voltage (DC)		–	300	V
$V_{GSO}$	gate-source voltage (DC)	open drain	–	$\pm 20$	V
$I_D$	drain current (DC)		–	350	mA
$I_{DM}$	peak drain current		–	1.4	A
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}; \text{note 1}$	–	1.5	W
$T_{stg}$	storage temperature		–55	+150	$^{\circ}\text{C}$
$T_j$	junction temperature		–	150	$^{\circ}\text{C}$

### Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm<sup>2</sup>.

# N-channel enhancement mode vertical D-MOS transistor

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## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient; note 1	83.3	K/W

### Note

1. Device mounted on an epoxy printed-circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm<sup>2</sup>.

## STATIC CHARACTERISTICS

$T_j = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10\ \mu\text{A}; V_{GS} = 0$	300	–	–	V
$I_{GSS}$	gate-source leakage current	$V_{GS} = \pm 20\ \text{V}; V_{DS} = 0$	–	–	$\pm 100$	nA
$V_{GSth}$	gate-source threshold voltage	$I_D = 1\ \text{mA}; V_{DS} = V_{GS}$	0.8	–	2	V
$R_{DSon}$	drain-source on-state resistance	$I_D = 20\ \text{mA}; V_{GS} = 2.4\ \text{V}$	–	4.8	10	$\Omega$
		$I_D = 250\ \text{mA}; V_{GS} = 10\ \text{V}$	–	3.7	6	$\Omega$
$I_{DSS}$	drain-source leakage current	$V_{DS} = 240\ \text{V}; V_{GS} = 0$	–	–	100	nA
$ Y_{fs} $	transfer admittance	$I_D = 250\ \text{mA}; V_{DS} = 25\ \text{V}$	200	690	–	mS
$C_{iss}$	input capacitance	$V_{DS} = 25\ \text{V}; V_{GS} = 0; f = 1\ \text{MHz}$	–	100	120	pF
$C_{oss}$	output capacitance	$V_{DS} = 25\ \text{V}; V_{GS} = 0; f = 1\ \text{MHz}$	–	21	30	pF
$C_{rss}$	feedback capacitance	$V_{DS} = 25\ \text{V}; V_{GS} = 0; f = 1\ \text{MHz}$	–	10	15	pF
<b>Switching times (see Figs 2 and 3)</b>						
$t_{on}$	turn-on time	$I_D = 250\ \text{mA}; V_{DD} = 50\ \text{V}; V_{GS} = 0\ \text{to}\ 10\ \text{V}$	–	6	10	ns
$t_{off}$	turn-off time	$I_D = 250\ \text{mA}; V_{DD} = 50\ \text{V}; V_{GS} = 10\ \text{to}\ 0\ \text{V}$	–	46	60	ns

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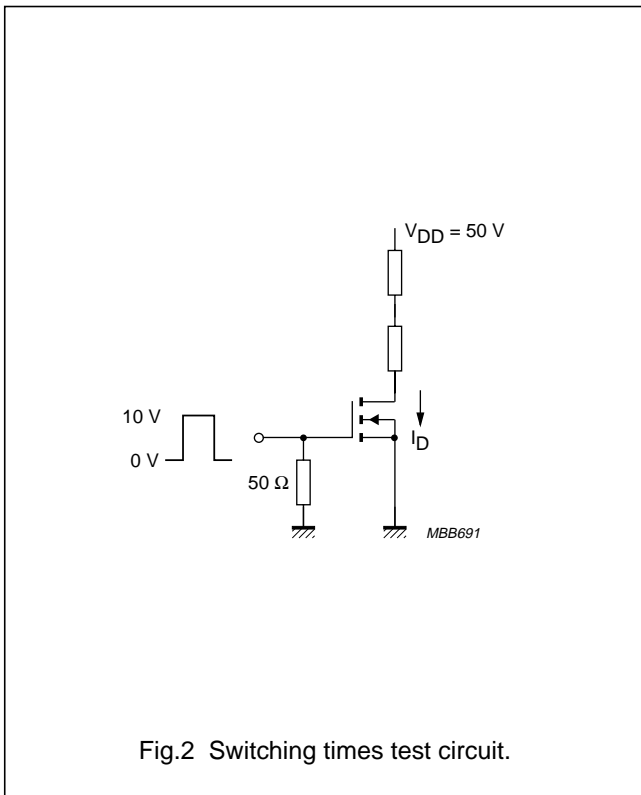


Fig.2 Switching times test circuit.

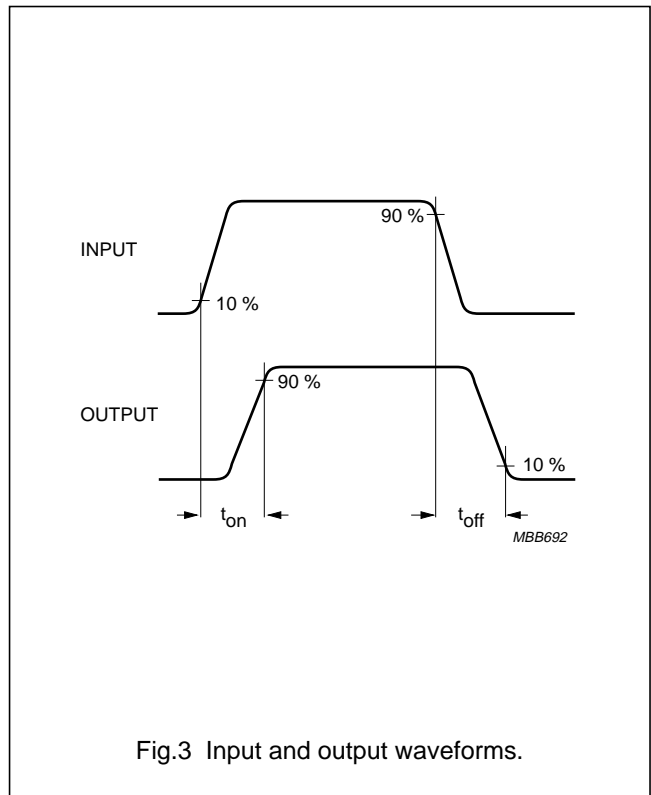


Fig.3 Input and output waveforms.

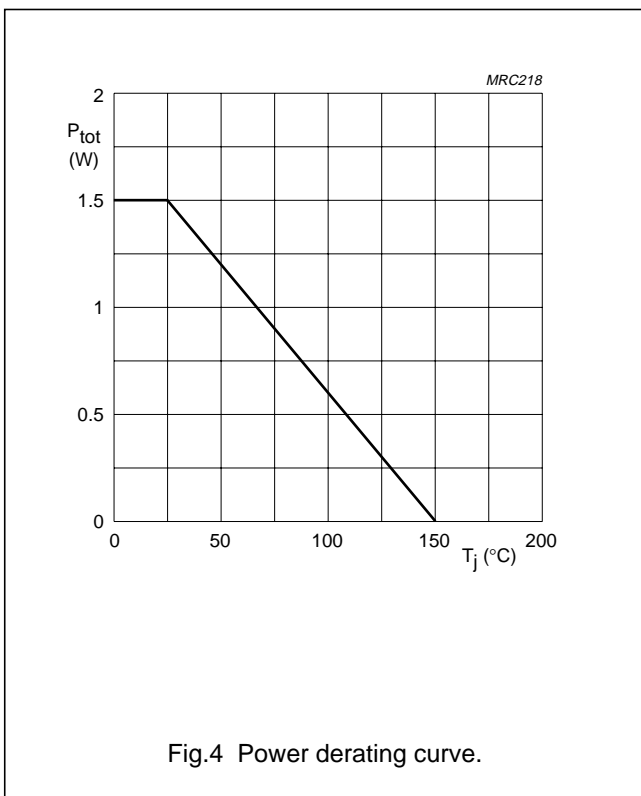
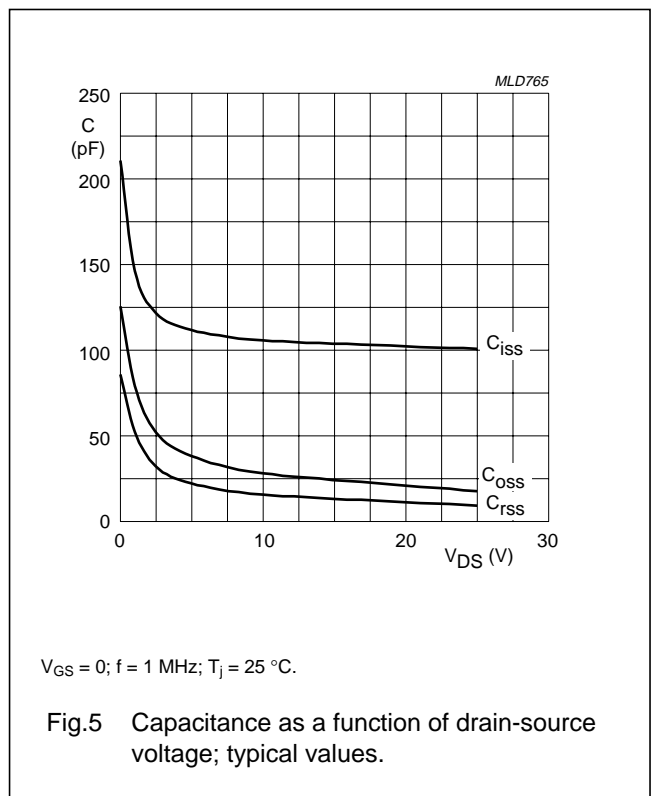


Fig.4 Power derating curve.

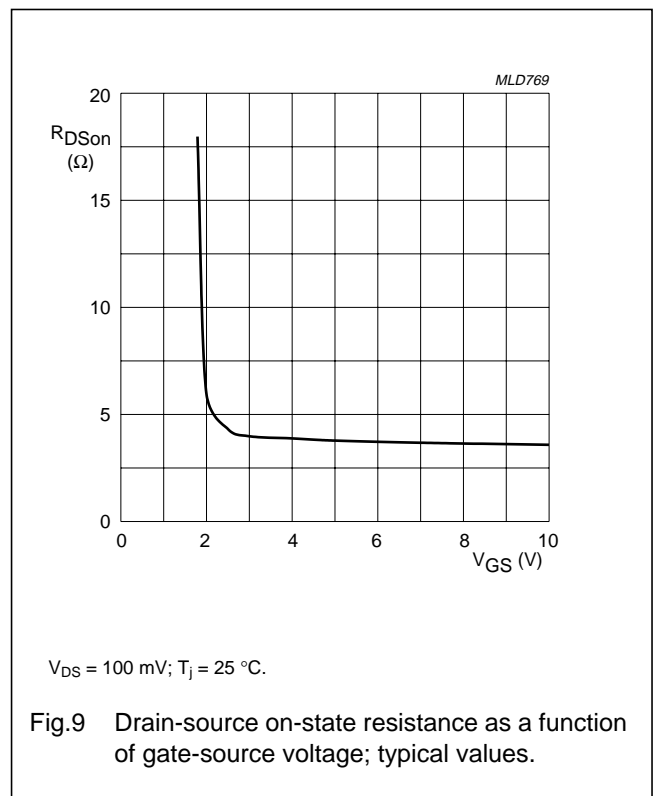
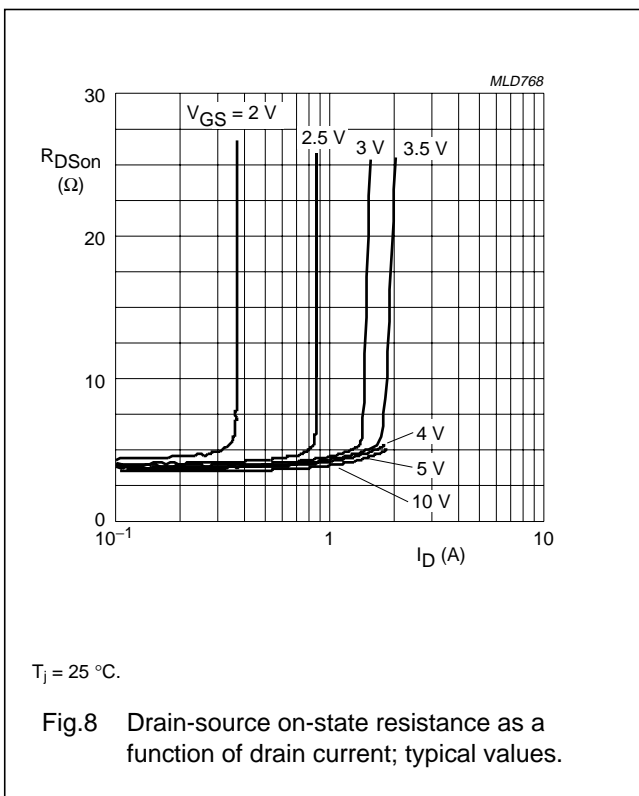
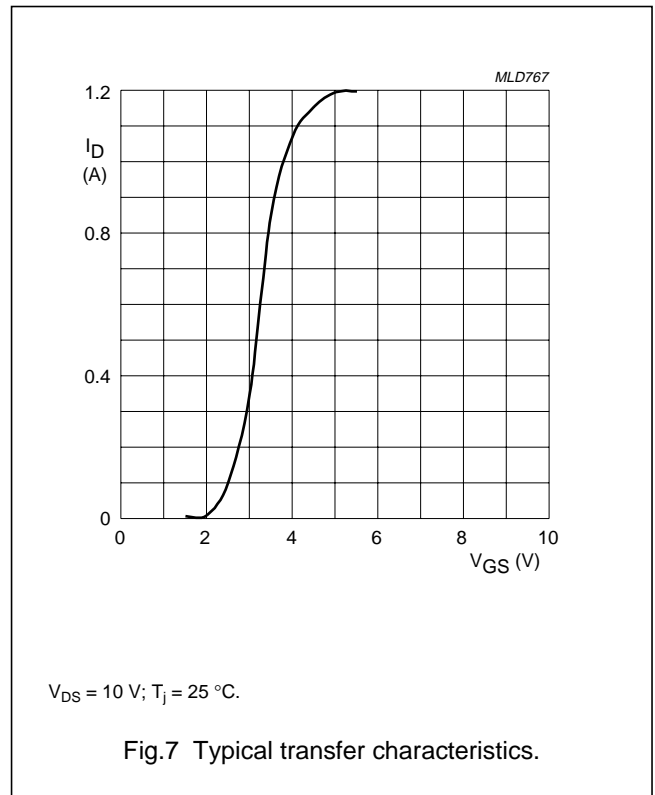
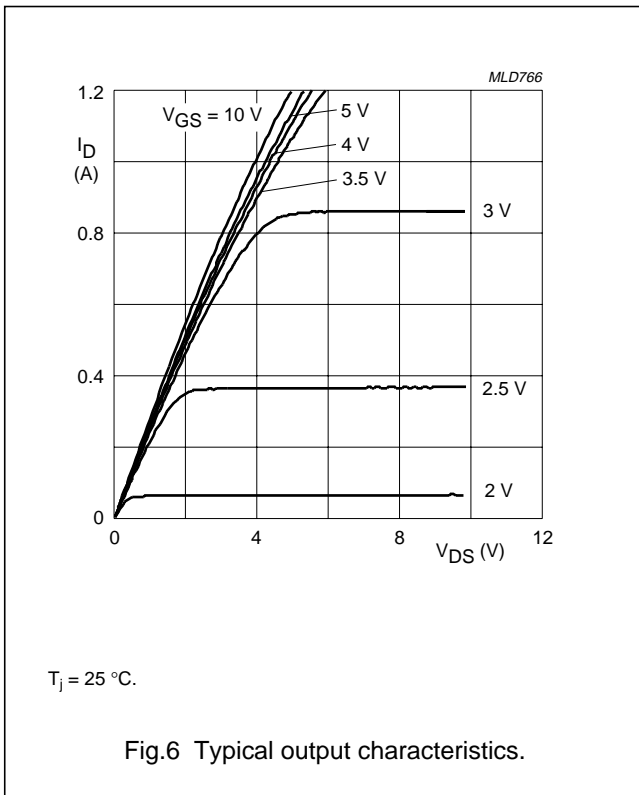


V<sub>GS</sub> = 0; f = 1 MHz; T<sub>j</sub> = 25 °C.

Fig.5 Capacitance as a function of drain-source voltage; typical values.

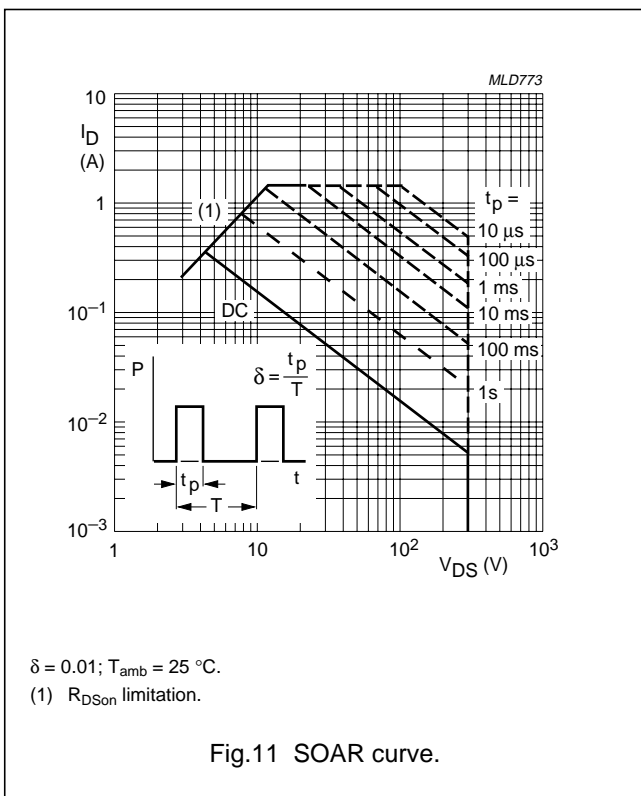
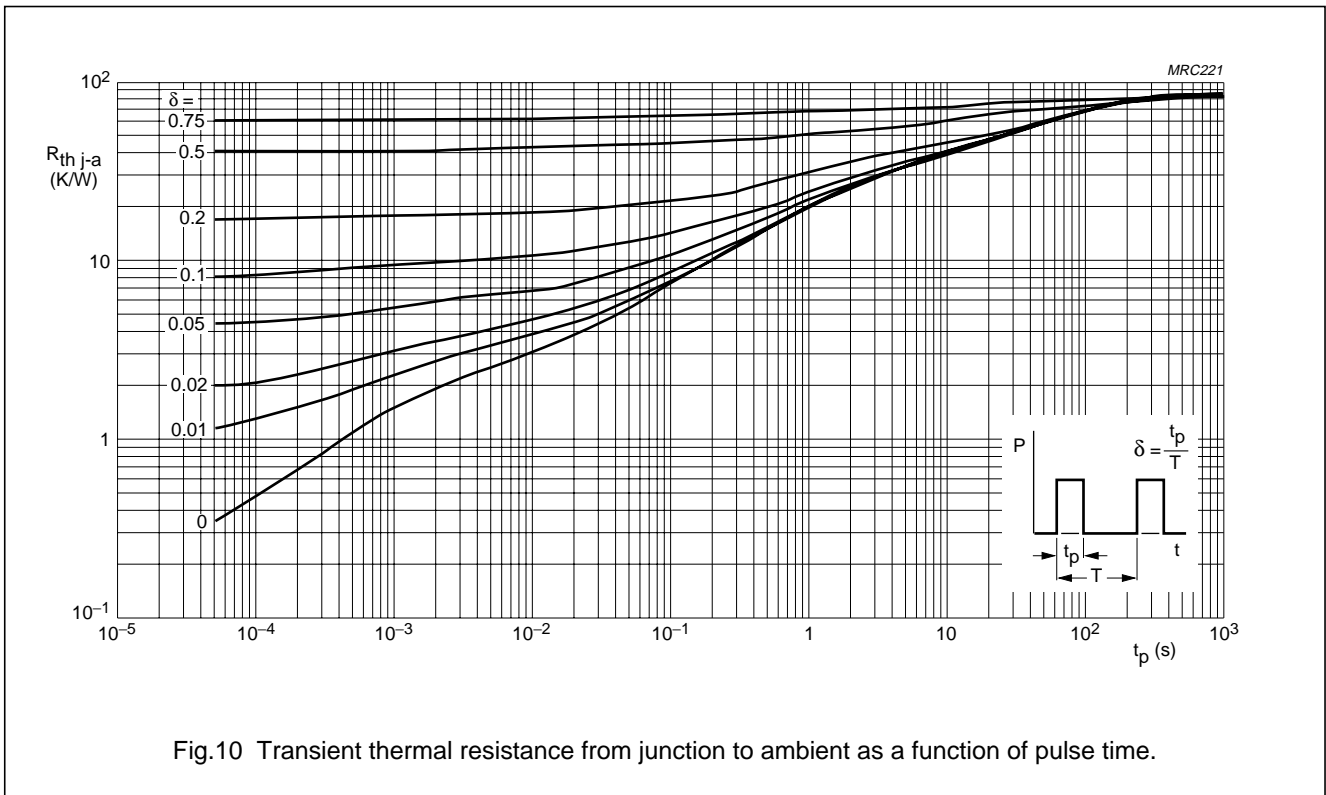
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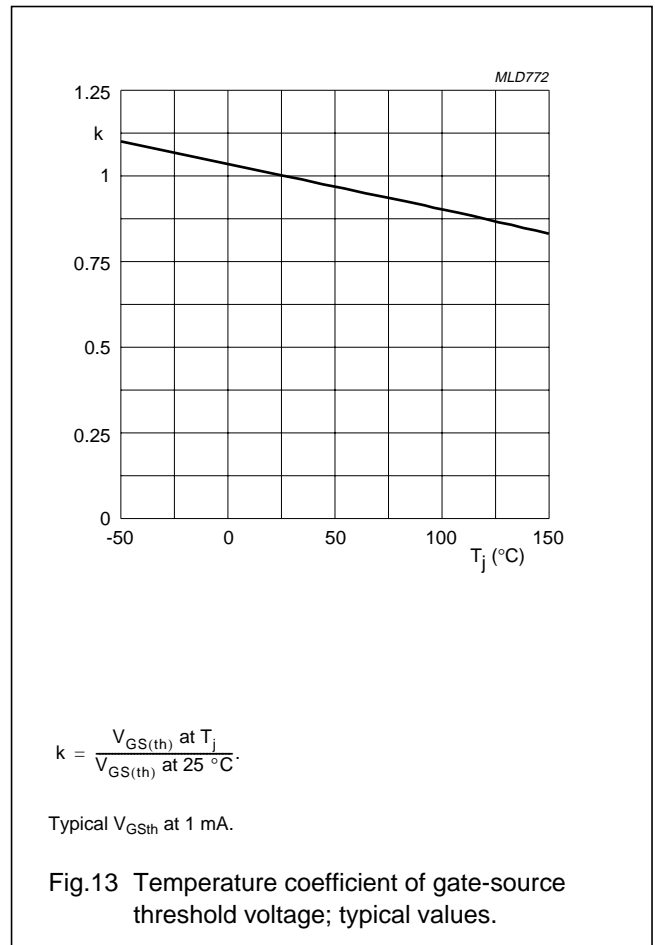
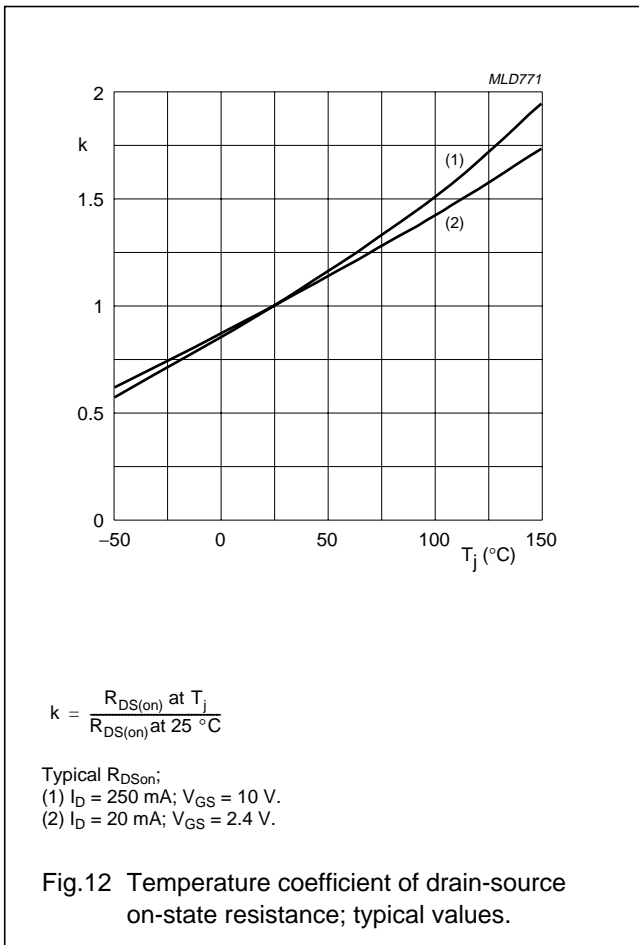
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N-channel enhancement mode vertical D-MOS transistor

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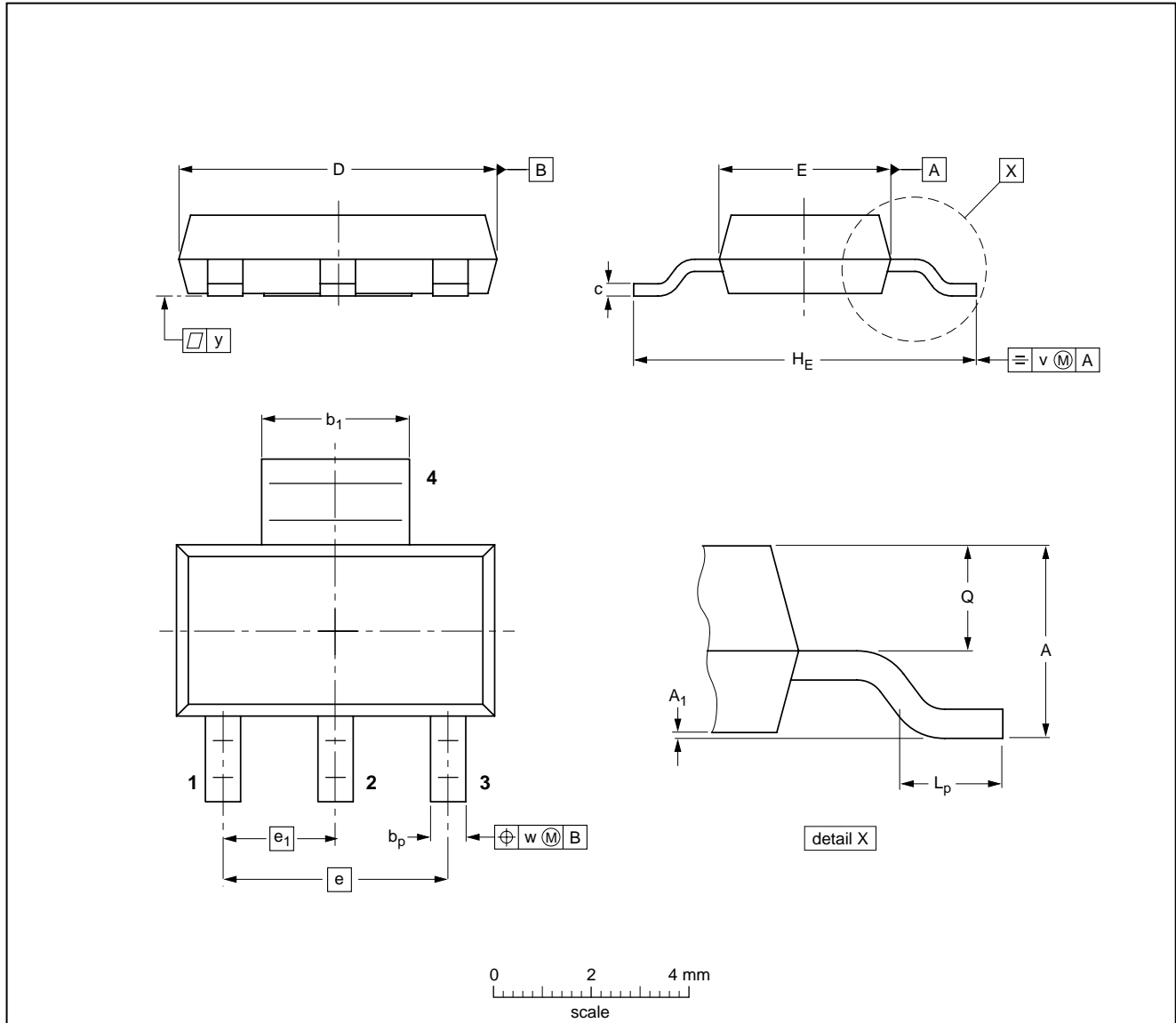
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PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b <sub>p</sub>	b <sub>1</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT223			SC-73		97-02-28 99-09-13



# N-channel enhancement mode vertical D-MOS transistor

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## DATA SHEET STATUS

DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITIONS
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**NOTES**

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**NOTES**

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## **Contact information**

For additional information please visit <http://www.semiconductors.philips.com>. Fax: +31 40 27 24825

For sales offices addresses send e-mail to: [sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com).

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Printed in The Netherlands

613510/03/pp12

Date of release: 2001 Dec 11

Document order number: 9397 750 09064

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