

BF904A; BF904AR; BF904AWR

N-channel dual gate MOS-FETs

Rev. 04 — 13 November 2007

Product data sheet

IMPORTANT NOTICE

Dear customer,

As from October 1st, 2006 Philips Semiconductors has a new trade name - NXP Semiconductors, which will be used in future data sheets together with new contact details.

In data sheets where the previous Philips references remain, please use the new links as shown below.

<http://www.philips.semiconductors.com> use <http://www.nxp.com>

<http://www.semiconductors.philips.com> use <http://www.nxp.com> (Internet)

sales.addresses@www.semiconductors.philips.com use salesaddresses@nxp.com (email)

The copyright notice at the bottom of each page (or elsewhere in the document, depending on the version)

- © Koninklijke Philips Electronics N.V. (year). All rights reserved -

is replaced with:

- © NXP B.V. (year). All rights reserved. -

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or phone (details via salesaddresses@nxp.com). Thank you for your cooperation and understanding,

NXP Semiconductors

N-channel dual gate MOS-FETs

BF904A; BF904AR; BF904AWR

FEATURES

- Specially designed for use at 5 V supply voltage
- Short channel transistor with high transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

- VHF and UHF applications with 3 to 7 V supply voltage such as television tuners and professional communications equipment.

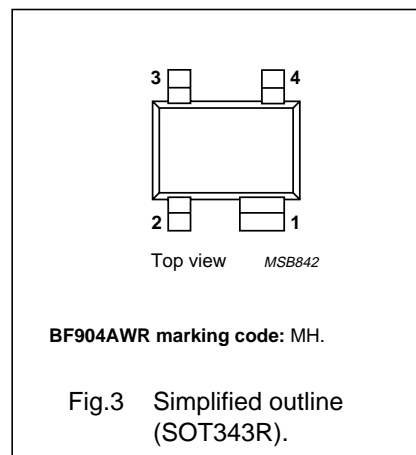
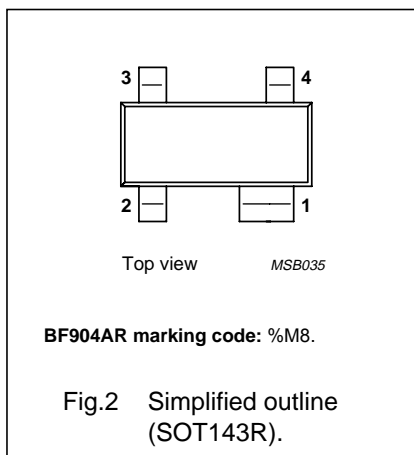
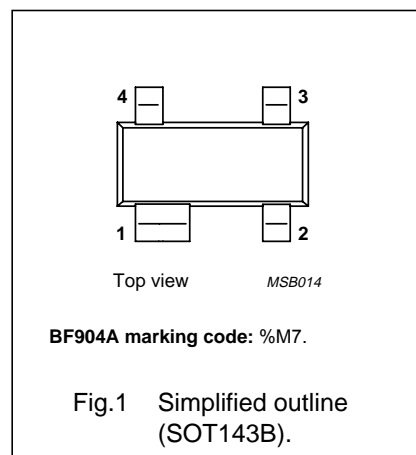
DESCRIPTION

Enhancement type field-effect transistors. The transistors consist of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

The BF904A, BF904AR and BF904AWR are encapsulated in the SOT143B, SOT143R and SOT343R plastic packages respectively.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	7	V
I_D	drain current		–	–	30	mA
P_{tot}	total power dissipation	$T_s \leq 110\text{ }^\circ\text{C}$	–	–	200	mW
$ y_{fs} $	forward transfer admittance		22	25	30	mS
C_{ig1-ss}	input capacitance at gate 1		–	2.2	2.6	pF
C_{rss}	reverse transfer capacitance	$f = 1\text{ MHz}$	–	25	35	fF
F	noise figure	$f = 800\text{ MHz}$	–	2	–	dB
T_j	operating junction temperature		–	–	150	$^\circ\text{C}$

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

N-channel dual gate MOS-FETs

BF904A; BF904AR; BF904AWR

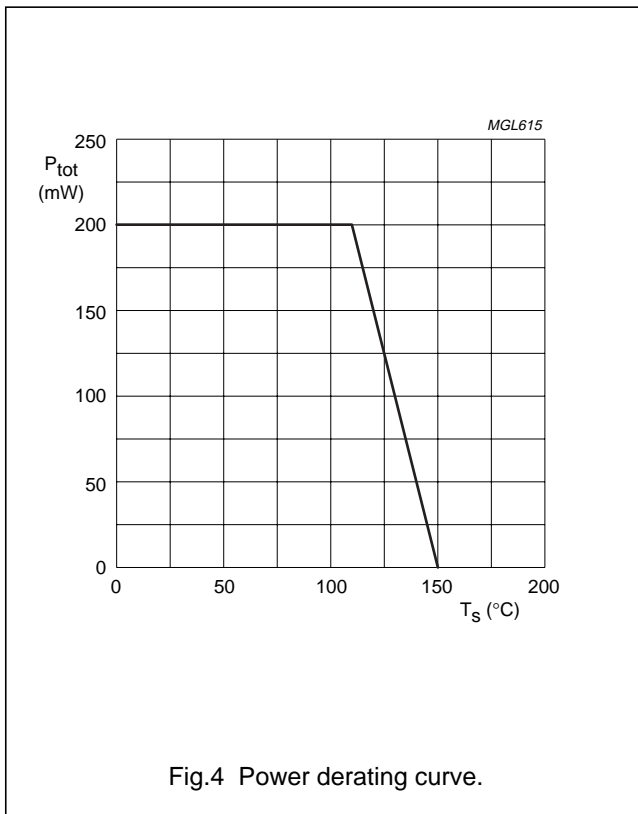
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{DS}	drain-source voltage		–	7	V
I _D	drain current		–	30	mA
I _{G1}	gate 1 current		–	±10	mA
I _{G2}	gate 2 current		–	±10	mA
P _{tot}	total power dissipation	T _s ≤ 110 °C; note 1; see Fig.4	–	200	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	operating junction temperature		–	150	°C

Note

1. T_s is the temperature of the soldering point of the source lead.



N-channel dual gate MOS-FETs

BF904A; BF904AR; BF904AWR

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	note 1	200	K/W

Note

- Soldering point of the source lead.

STATIC CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0$; $I_{G1-S} = 10\text{ mA}$	6	15	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$; $I_{G2-S} = 10\text{ mA}$	6	15	V
$V_{(F)S-G1}$	forward source-gate 1 voltage	$V_{G2-S} = V_{DS} = 0$; $I_{S-G1} = 10\text{ mA}$	0.5	1.5	V
$V_{(F)S-G2}$	forward source-gate 2 voltage	$V_{G1-S} = V_{DS} = 0$; $I_{S-G2} = 10\text{ mA}$	0.5	1.5	V
$V_{G1-S(th)}$	gate 1-source threshold voltage	$V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $I_D = 20\text{ }\mu\text{A}$	0.3	1	V
$V_{G2-S(th)}$	gate 2-source threshold voltage	$V_{G1-S} = V_{DS} = 5\text{ V}$; $I_D = 20\text{ }\mu\text{A}$	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $R_{G1} = 120\text{ k}\Omega$; note 1	8	13	mA
I_{G1-SS}	gate 1 cut-off current	$V_{G2-S} = V_{DS} = 0$; $V_{G1-S} = 5\text{ V}$	–	50	nA
I_{G2-SS}	gate 2 cut-off current	$V_{G1-S} = V_{DS} = 0$; $V_{G2-S} = 5\text{ V}$	–	50	nA

Note

- R_{G1} connects gate 1 to $V_{GG} = 5\text{ V}$; see Fig.21.

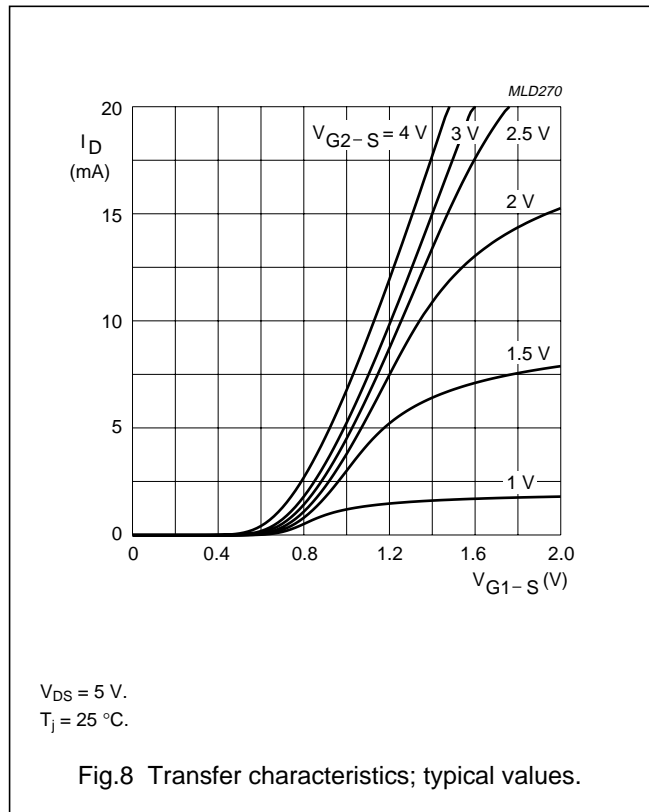
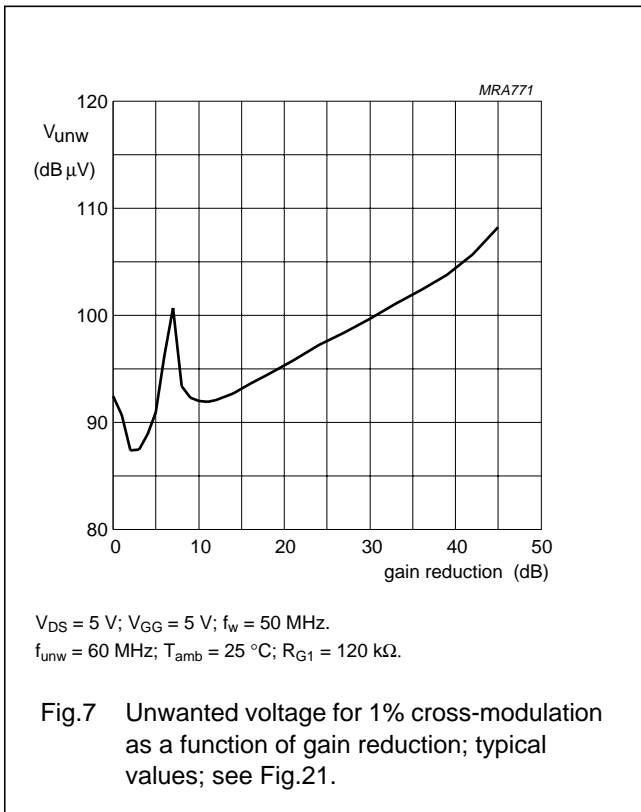
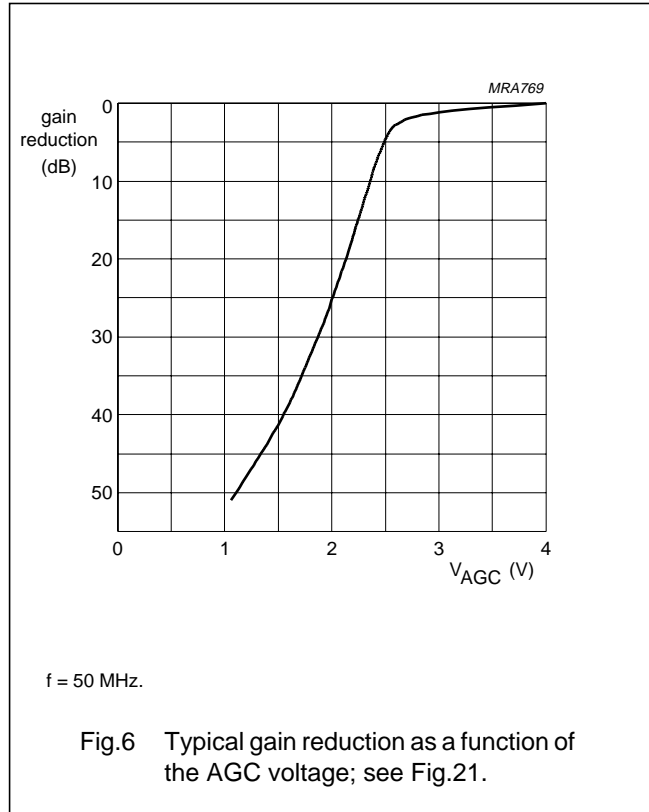
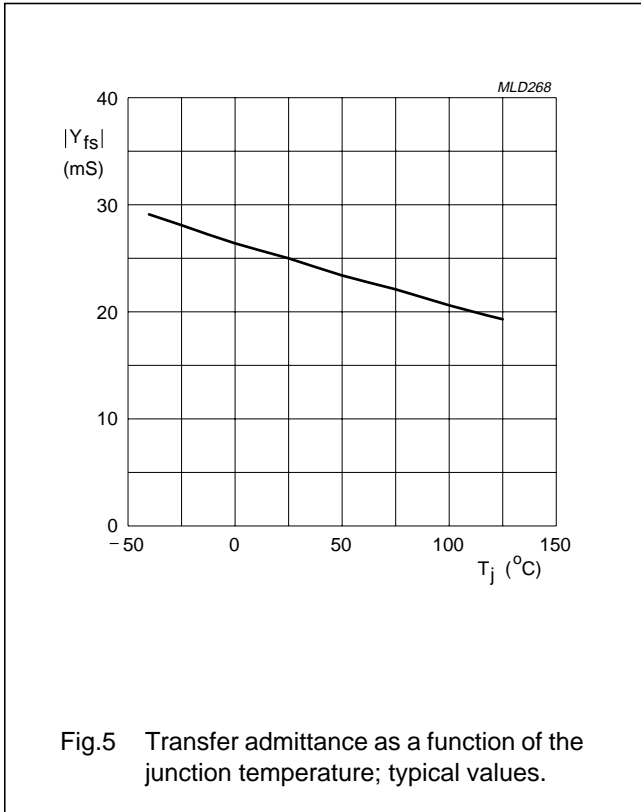
DYNAMIC CHARACTERISTICS

Common source; $T_{amb} = 25\text{ °C}$; $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 10\text{ mA}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{fs} $	forward transfer admittance	pulsed; $T_j = 25\text{ °C}$	22	25	30	mS
C_{ig1-s}	input capacitance at gate 1	$f = 1\text{ MHz}$	–	2.2	2.6	pF
C_{ig2-s}	input capacitance at gate 2	$f = 1\text{ MHz}$	1	1.5	2	pF
C_{os}	drain-source capacitance	$f = 1\text{ MHz}$	1	1.4	1.7	pF
C_{rs}	reverse transfer capacitance	$f = 1\text{ MHz}$	–	25	35	fF
F	noise figure	$f = 200\text{ MHz}$; $G_S = 2\text{ mS}$; $B_S = B_{Sopt}$	–	1	1.5	dB
		$f = 800\text{ MHz}$; $G_S = G_{Sopt}$; $B_S = B_{Sopt}$	–	2	2.8	dB

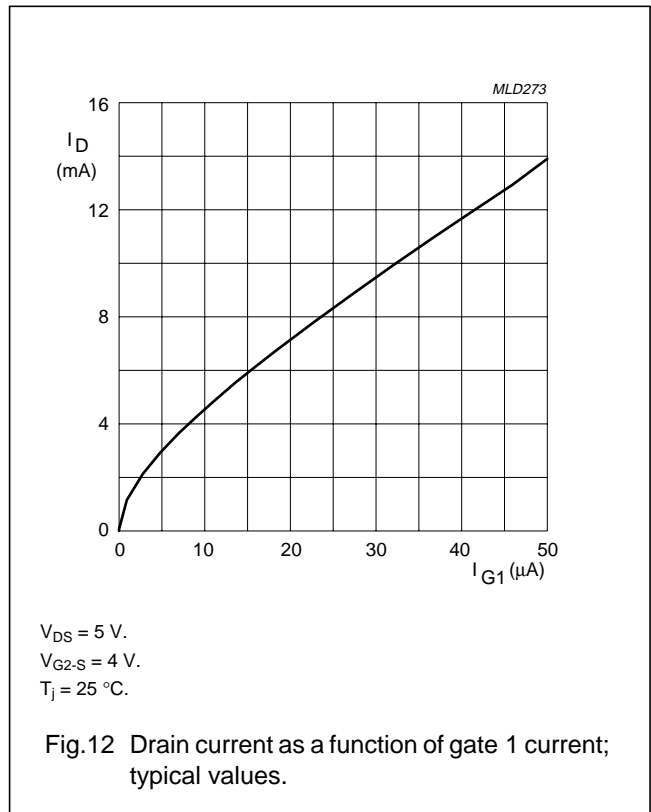
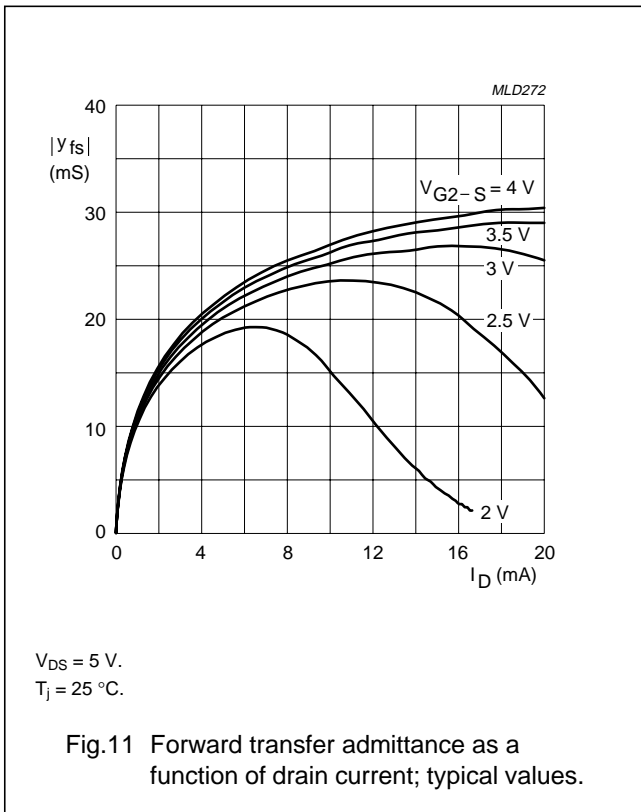
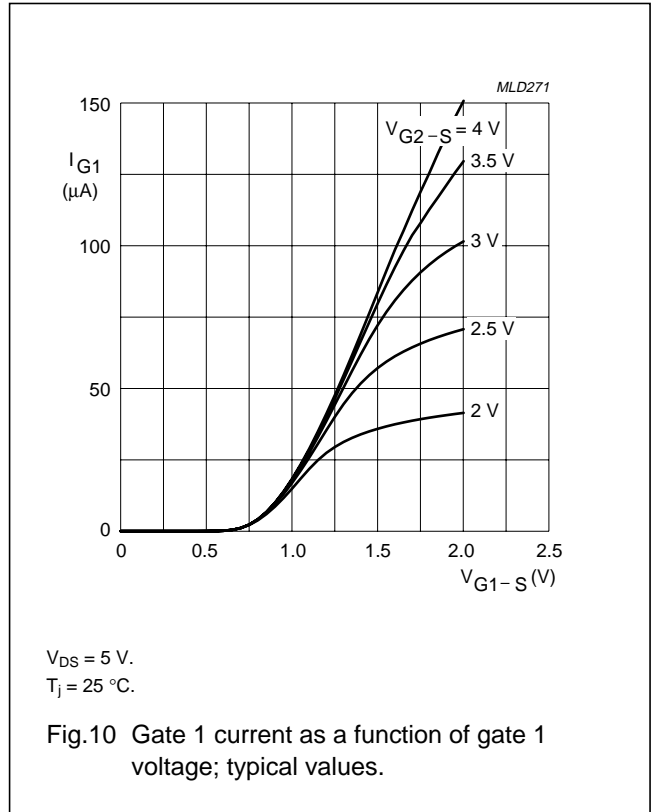
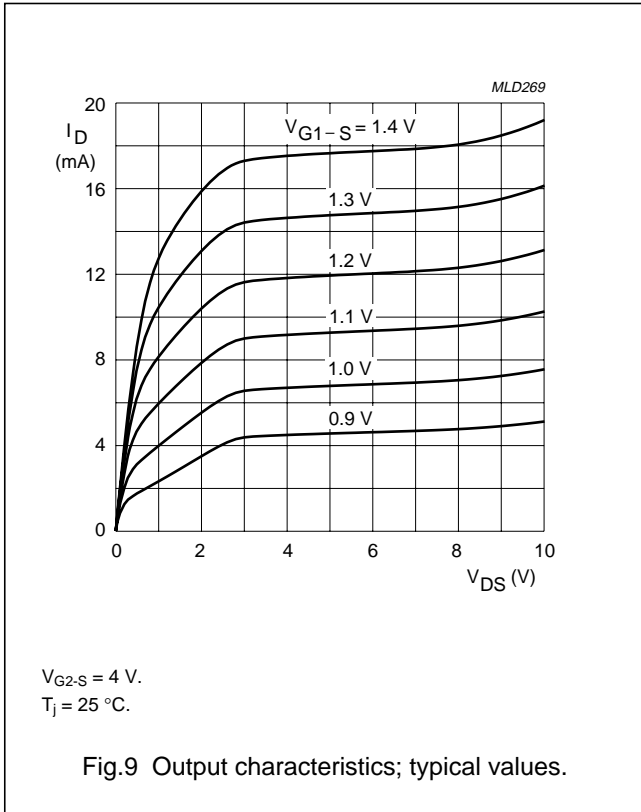
N-channel dual gate MOS-FETs

BF904A; BF904AR; BF904AWR



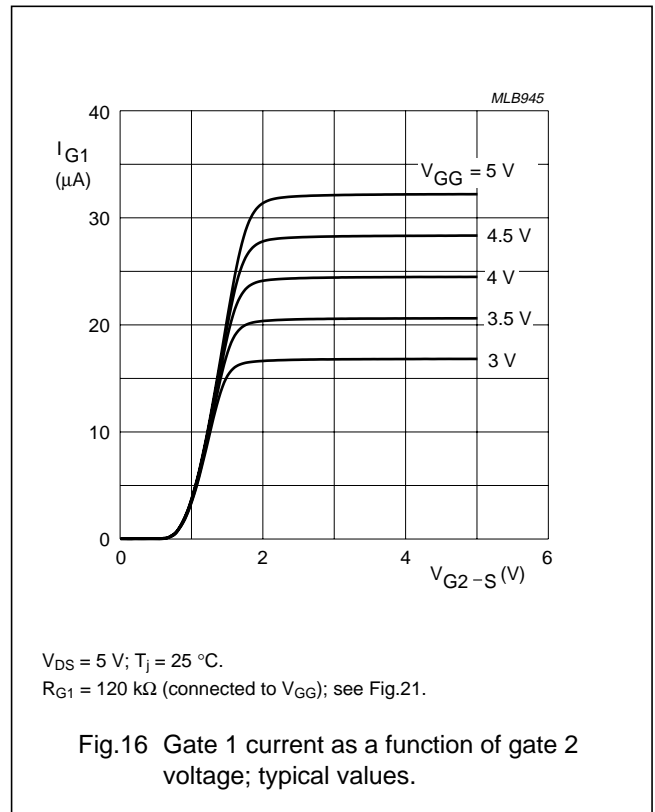
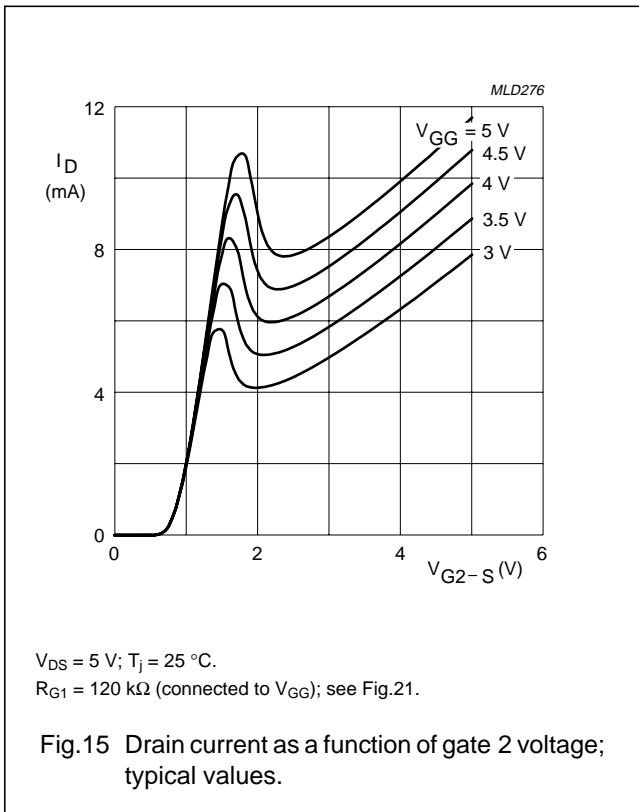
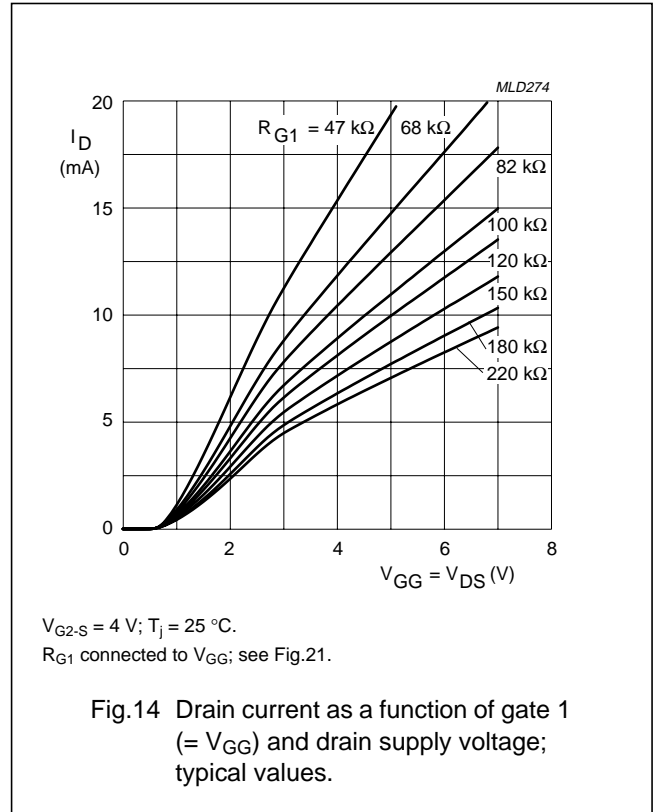
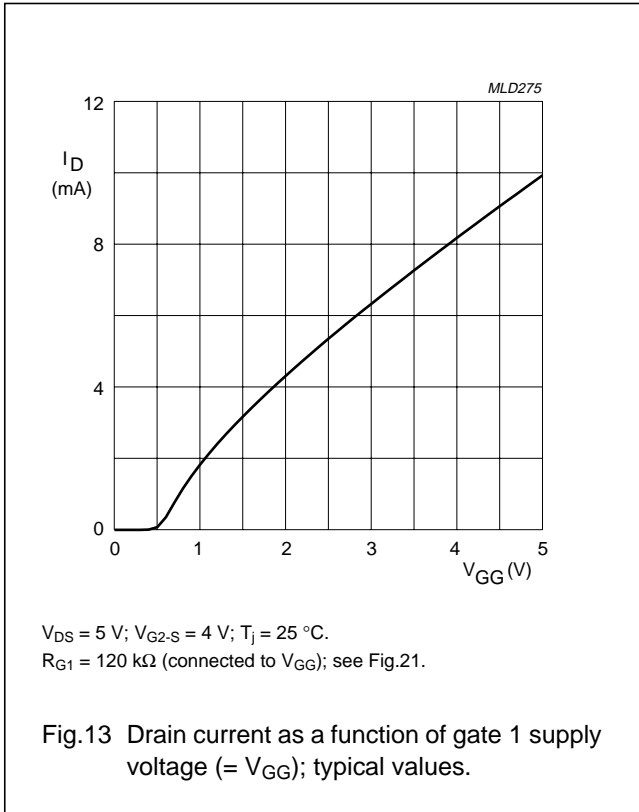
N-channel dual gate MOS-FETs

BF904A; BF904AR; BF904AWR



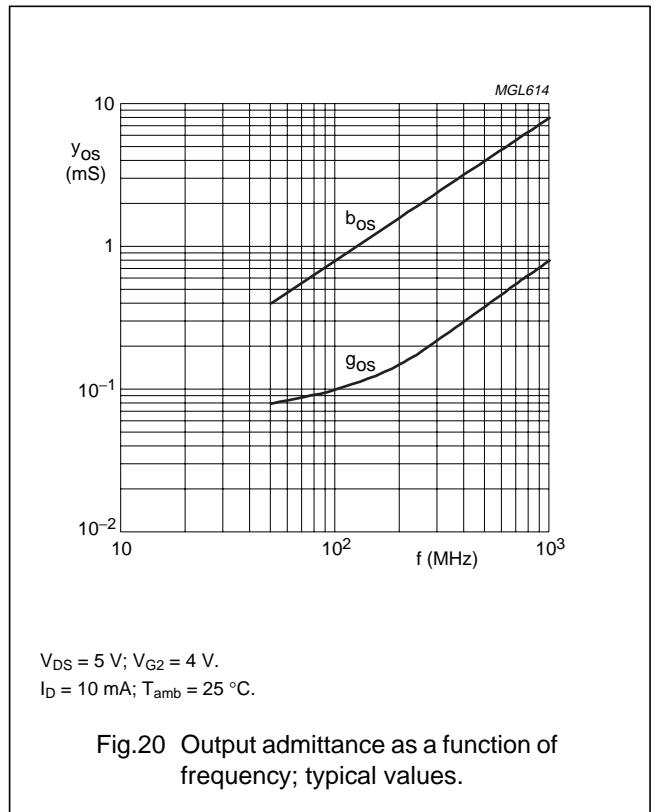
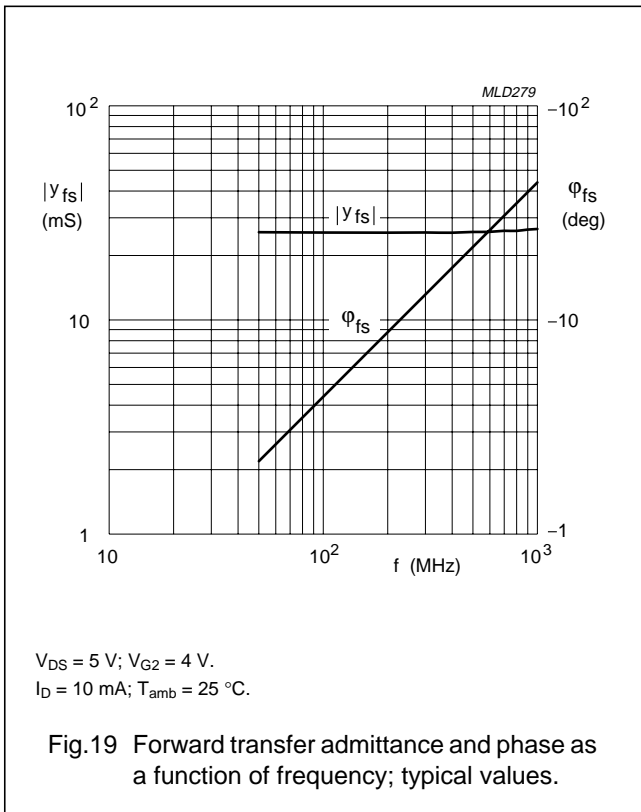
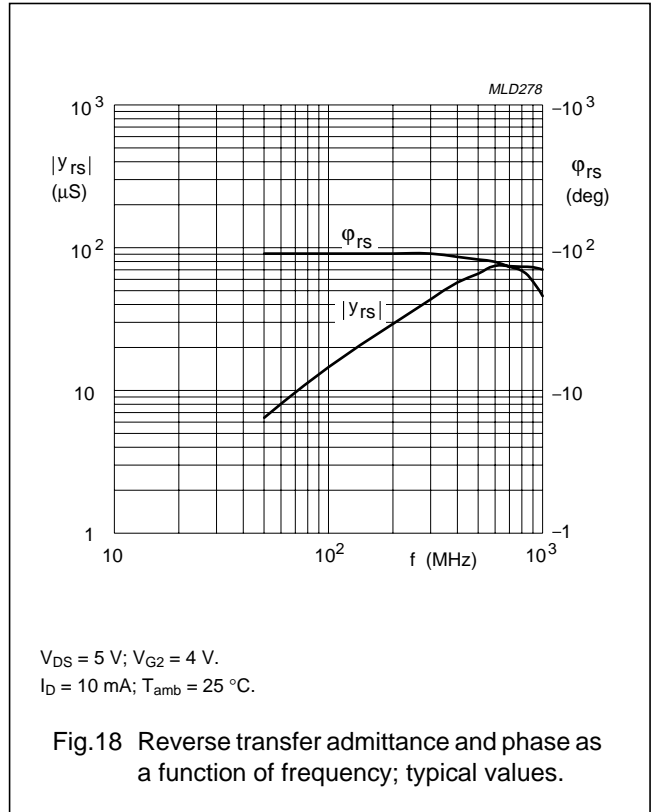
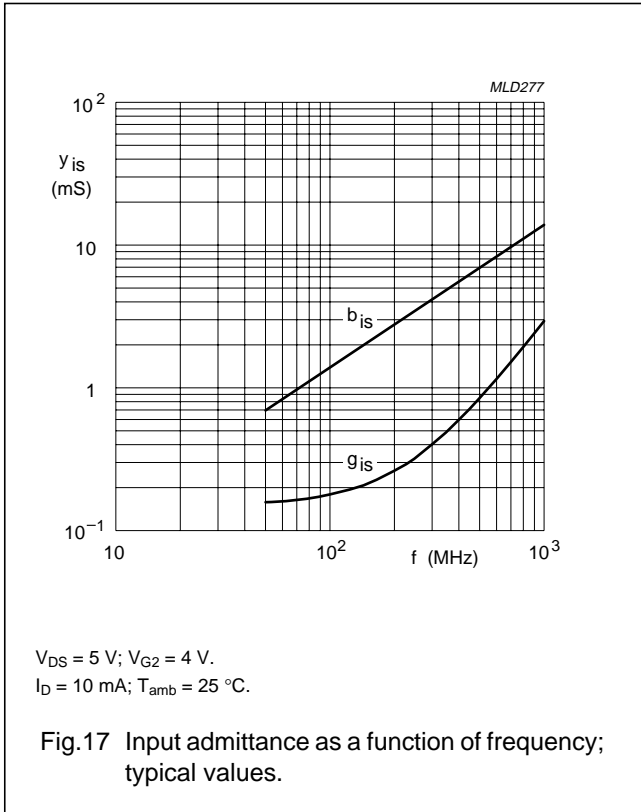
N-channel dual gate MOS-FETs

BF904A; BF904AR; BF904AWR



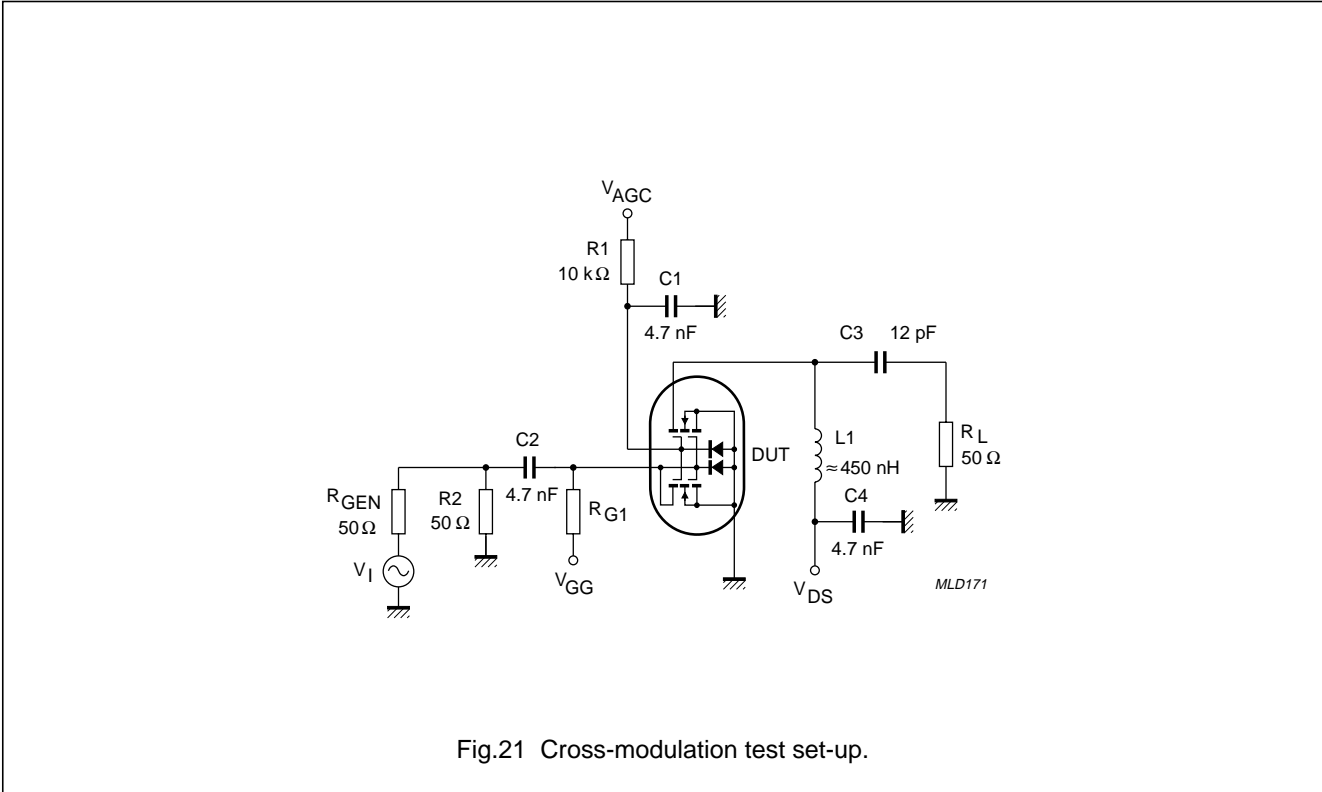
N-channel dual gate MOS-FETs

BF904A; BF904AR; BF904AWR



N-channel dual gate MOS-FETs

BF904A; BF904AR; BF904AWR



N-channel dual gate MOS-FETs

BF904A; BF904AR; BF904AWR

Table 1 Scattering parameters: $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 10\text{ mA}$; $T_{amb} = 25\text{ °C}$

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
40	0.989	-3.2	2.52	175.9	0.001	87.9	0.989	-1.7
100	0.987	-7.9	2.52	169.4	0.001	86.1	0.988	-4.3
200	0.976	-15.7	2.47	159.2	0.003	81.4	0.984	-8.6
300	0.972	-23.3	2.43	150.5	0.004	80.5	0.985	-12.7
400	0.947	-30.6	2.36	139.6	0.005	76.9	0.975	-16.9
500	0.925	-37.6	2.26	130.3	0.005	75.6	0.968	-20.8
600	0.905	-44.4	2.19	121.1	0.005	75.5	0.961	-24.7
700	0.883	-50.9	2.10	112.3	0.006	78.0	0.954	-28.4
800	0.861	-57.0	2.01	103.6	0.006	85.3	0.946	-32.0
900	0.841	-63.0	1.93	95.5	0.006	90.7	0.934	-35.6
1000	0.822	-68.4	1.85	87.8	0.006	102.6	0.931	-39.3
1200	0.787	-78.9	1.71	72.3	0.007	127.1	0.923	-46.7
1400	0.752	-88.1	1.59	57.3	0.011	143.7	0.926	-54.2
1600	0.723	-97.3	1.47	40.1	0.019	150.0	0.935	-62.2
1800	0.685	-106.3	1.36	25.0	0.021	149.4	0.931	-69.3
2000	0.665	-114.0	1.31	7.7	0.026	151.5	0.930	-77.7
2200	0.659	-119.8	1.30	-14.0	0.035	158.2	0.944	-89.1
2400	0.670	-124.2	1.26	-42.2	0.050	163.4	0.941	-103.5
2600	0.700	-129.3	1.10	-78.2	0.076	162.2	0.849	-119.7
2800	0.729	-138.7	0.82	-120.8	0.106	150.5	0.642	-130.9
3000	0.726	-150.1	0.52	-162.8	0.128	137.4	0.480	-130.6

Table 2 Noise data: $V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 10\text{ mA}$; $T_{amb} = 25\text{ °C}$

f (MHz)	F _{min} (dB)	Γ _{opt}		R _n (Ω)
		(ratio)	(deg)	
800	2.0	0.686	49.6	50.4

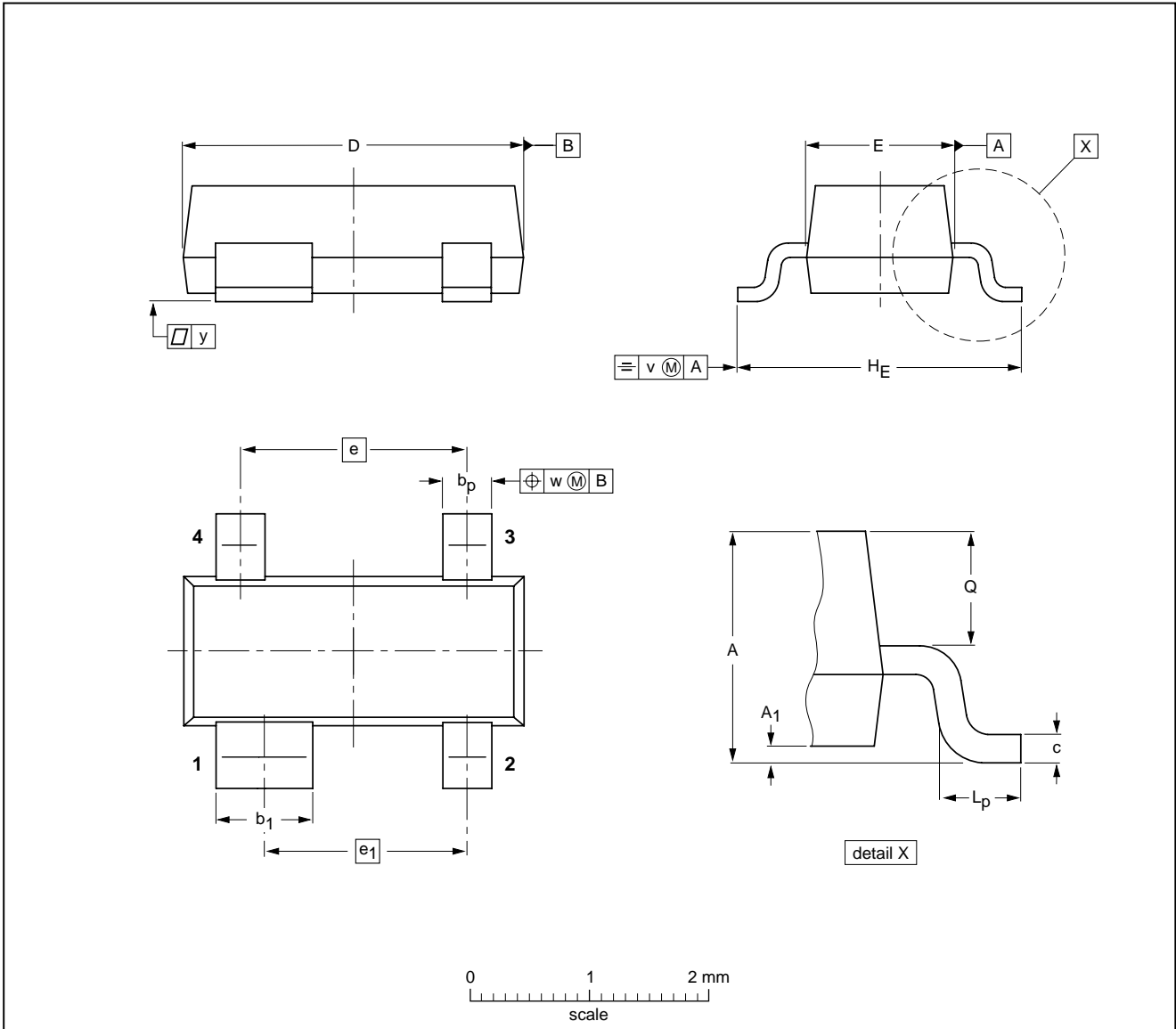
N-channel dual gate MOS-FETs

BF904A; BF904AR; BF904AWR

PACKAGE OUTLINES

Plastic surface mounted package; 4 leads

SOT143B



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

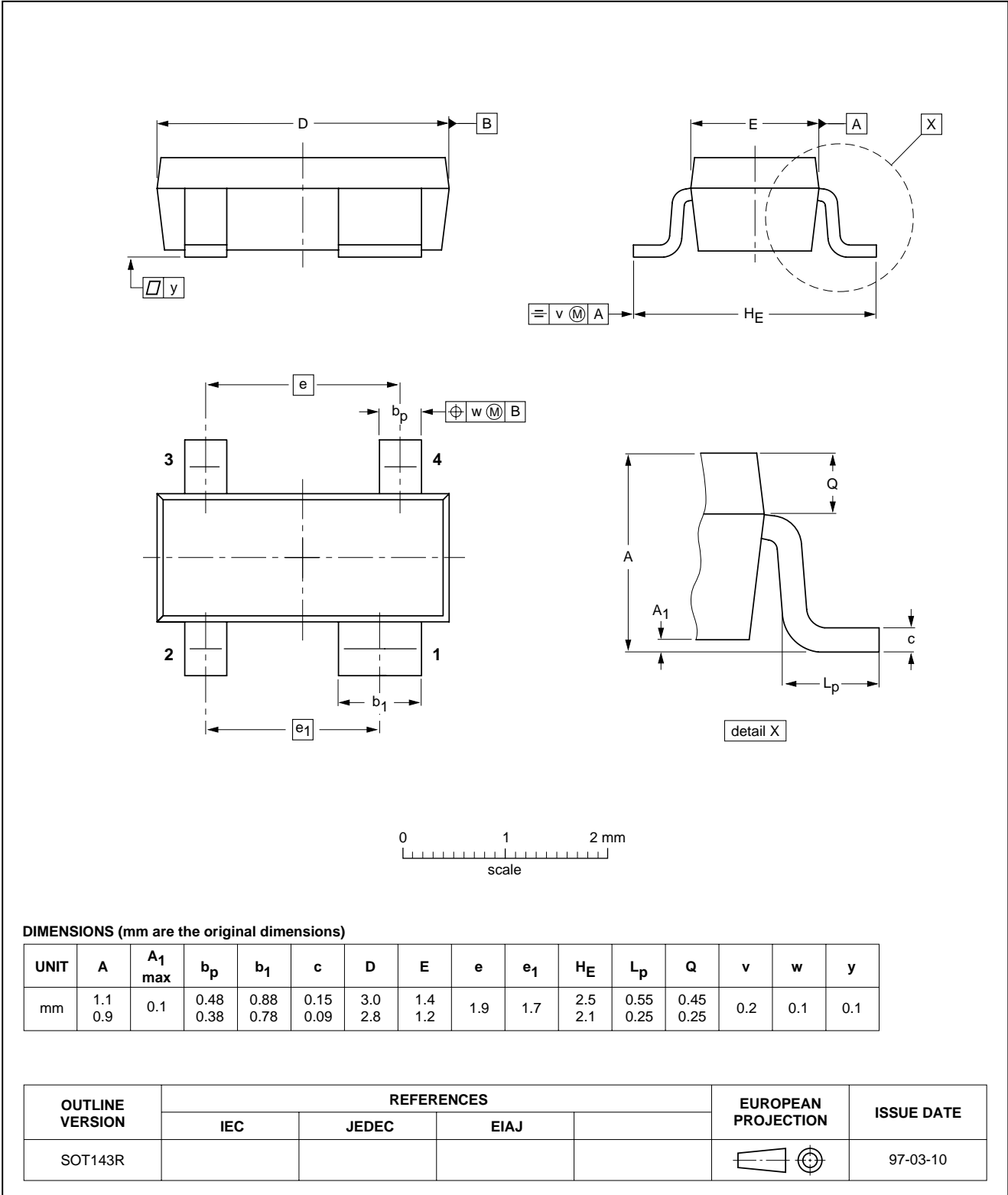
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT143B						97-02-28

N-channel dual gate MOS-FETs

BF904A; BF904AR; BF904AWR

Plastic surface mounted package; reverse pinning; 4 leads

SOT143R

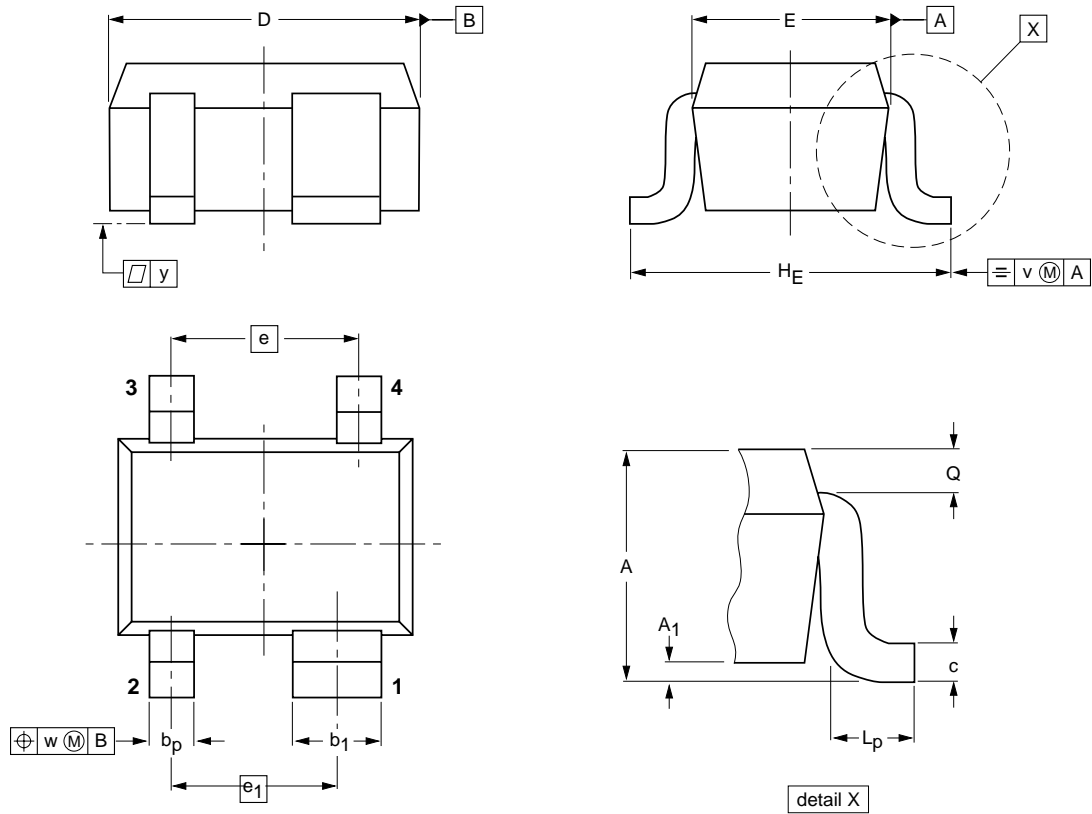


N-channel dual gate MOS-FETs

BF904A; BF904AR; BF904AWR

Plastic surface mounted package; reverse pinning; 4 leads

SOT343R



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						97-05-21

Legal information

Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contact information

For additional information, please visit: <http://www.nxp.com>

For sales office addresses, send an email to: salesaddresses@nxp.com

Revision history

Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BF904A_AR_AWR_N_4	20071113	Product data sheet	-	BF904A_AR_AWR_3
Modifications:	<ul style="list-style-type: none"> • Fig. 1 and 2 on page 2; Figure note changed 			
BF904A_AR_AWR_3 (9397 750 05271)	19990514	Product specification	-	BF904A_AR_AWR_N_2
BF904A_AR_AWR_N_2 (9397 750 05234)	19990201	Preliminary specification	-	BF904A_AR_AWR_N_1
BF904A_AR_AWR_N_1 (9397 750 04748)	19981130	Preliminary specification	-	-

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2007.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 13 November 2007

Document identifier: BF904A_AR_AWR_N_4