

PSMN020-30MLC

N-channel 30 V 18.1 mΩ logic level MOSFET in LFPAK33 using TrenchMOS Technology

4 September 2012

Product data sheet

1. Product profile

1.1 General description

Logic level enhancement mode N-channel MOSFET in LFPAK33 package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- Low parasitic inductance and resistance
- Optimised for 4.5V Gate drive utilising Superjunction technology
- Ultra low QG, QGD, and QOSS for high system efficiencies at low and high loads

1.3 Applications

- DC-to-DC converters
- Load switching
- Synchronous buck regulator

1.4 Quick reference data

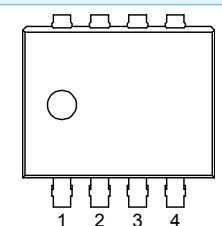
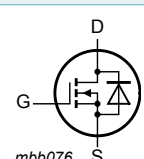
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ }^\circ\text{C}$	-	-	30	V
I_D	drain current	$T_{mb} = 25\text{ }^\circ\text{C}$; $V_{GS} = 10\text{ V}$; Fig. 1	-	-	31.8	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 2	-	-	33	W
T_j	junction temperature		-55	-	175	$^\circ\text{C}$
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}$; $I_D = 5\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10	-	20.5	27	mΩ
		$V_{GS} = 10\text{ V}$; $I_D = 5\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10	-	14.7	18.1	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5\text{ V}$; $I_D = 5\text{ A}$; $V_{DS} = 15\text{ V}$; Fig. 12 ; Fig. 13	-	1.7	-	nC
$Q_{G(tot)}$	total gate charge	$V_{GS} = 4.5\text{ V}$; $I_D = 5\text{ A}$; $V_{DS} = 15\text{ V}$; Fig. 12 ; Fig. 13	-	4.6	-	nC



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LFAK33 (SOT1210)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PSMN020-30MLC	LFAK33	Plastic single ended surface mounted package (LFAK33); 4 leads	SOT1210

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	31.8	A
		$V_{GS} = 10\text{ V}; T_{mb} = 100\text{ °C}; \text{Fig. 1}$	-	22.5	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25\text{ °C}; \text{Fig. 4}$	-	127	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 2}$	-	33	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C
V_{ESD}	electrostatic discharge voltage	MM (JEDEC JESD22-A115)	130	-	V
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	27.4	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25\text{ °C}$	-	127	A

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Symbol	Parameter	Conditions	Min	Max	Unit
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25\text{ }^\circ\text{C}; I_D = 31\text{ A}; V_{\text{sup}} \leq 30\text{ V}; R_{GS} = 50\text{ }\Omega$; unclamped; Fig. 3	-	7.7	mJ

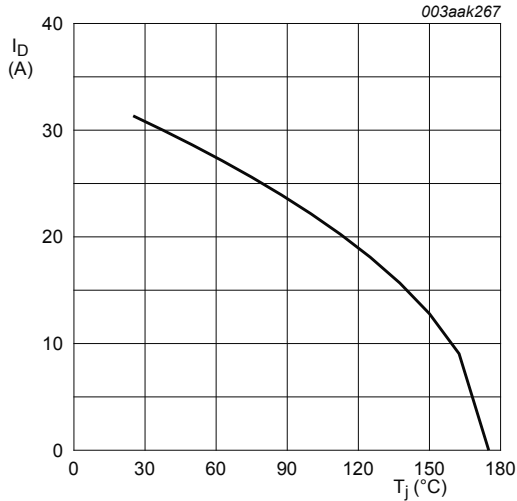


Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10V$$

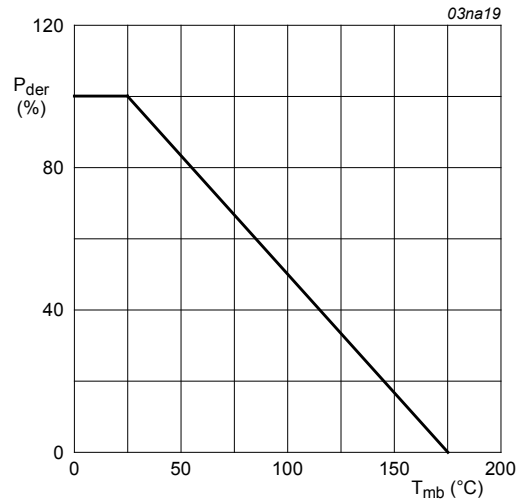


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

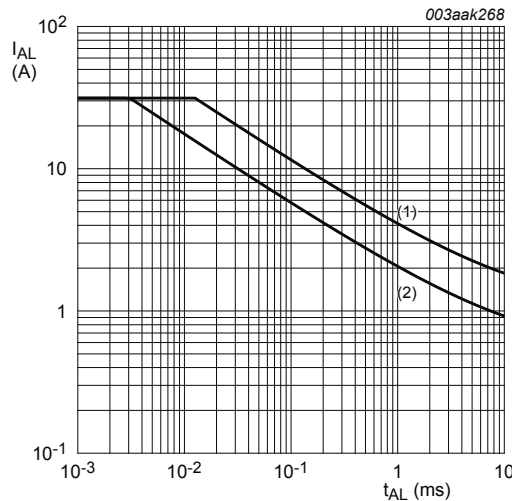


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j(\text{init})} = 25^\circ\text{C}$; (2) $T_{j(\text{init})} = 100^\circ\text{C}$

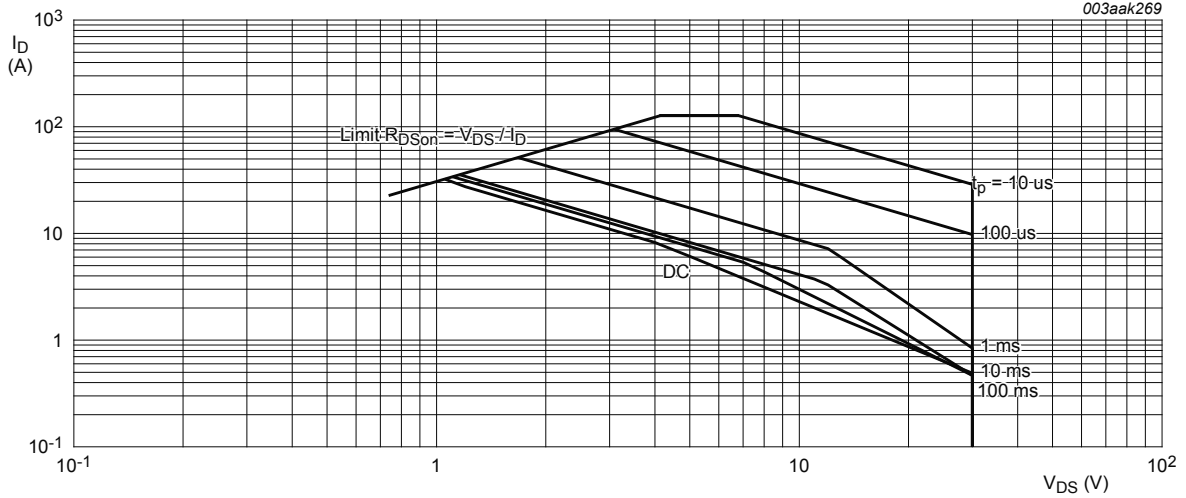


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	4.32	4.56	K/W

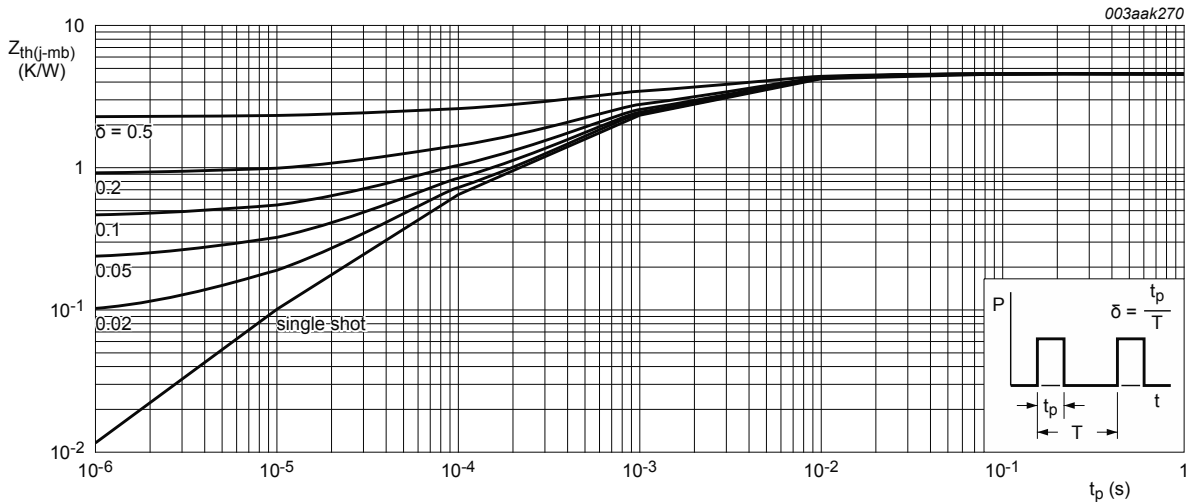


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 13.5 \text{ A}; V_{GS} = 0 \text{ V}; T_{j(\text{init})} = 25 \text{ }^\circ\text{C}; t_p \leq 50 \text{ } \mu\text{s}$	34	-	-	V
		$I_D = 250 \text{ } \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	30	-	-	V
		$I_D = 250 \text{ } \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	27	-	-	V
$V_{GS(\text{th})}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	1.05	1.62	1.95	V
$\Delta V_{GS(\text{th})}/\Delta T$	gate-source threshold voltage variation with temperature		-	-3.5	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	1	μA
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 10	-	20.5	27	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 5 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ Fig. 10; Fig. 11	-	-	43.2	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 10	-	14.7	18.1	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ Fig. 10; Fig. 11	-	-	29	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}$	0.68	1.37	2.74	Ω
Dynamic characteristics						
$Q_{G(\text{tot})}$	total gate charge	$I_D = 5 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 12; Fig. 13	-	9.5	-	nC
		$I_D = 5 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$ Fig. 12; Fig. 13	-	4.6	-	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	8.4	-	nC
Q_{GS}	gate-source charge	$I_D = 5 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 4.5 \text{ V};$ Fig. 12; Fig. 13	-	1	-	nC
$Q_{GS(\text{th})}$	pre-threshold gate-source charge		-	0.3	-	nC
$Q_{GS(\text{th-pl})}$	post-threshold gate-source charge		-	0.7	-	nC
Q_{GD}	gate-drain charge		-	1.7	-	nC
$V_{GS(\text{pl})}$	gate-source plateau voltage	$I_D = 5 \text{ A}; V_{DS} = 15 \text{ V};$ Fig. 12; Fig. 13	-	2.4	-	V

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{iss}	input capacitance	$V_{DS} = 15\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C};$ Fig. 14	-	430	-	pF
C_{oss}	output capacitance		-	120	-	pF
C_{rss}	reverse transfer capacitance		-	70	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15\text{ V}; R_L = 3\text{ } \Omega; V_{GS} = 4.5\text{ V}; R_{G(ext)} = 5\text{ } \Omega$	-	6.1	-	ns
t_r	rise time		-	7.2	-	ns
$t_{d(off)}$	turn-off delay time		-	10.1	-	ns
t_f	fall time		-	5.1	-	ns
Q_{oss}	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 15\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C}$	-	2.3	-	nC
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 5\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 15	-	0.89	1.1	V
t_{rr}	reverse recovery time	$I_S = 5\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 15\text{ V}$	-	13.5	-	ns
Q_r	recovered charge		-	5.1	-	nC
t_a	reverse recovery rise time	$V_{GS} = 0\text{ V}; I_S = 5\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{DS} = 15\text{ V};$ Fig. 16	-	6.3	-	ns
t_b	reverse recovery fall time		-	7.2	-	ns

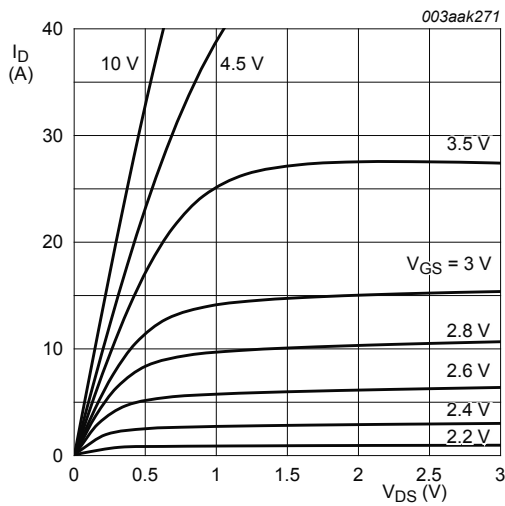


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

$T_j = 25^\circ\text{C}$

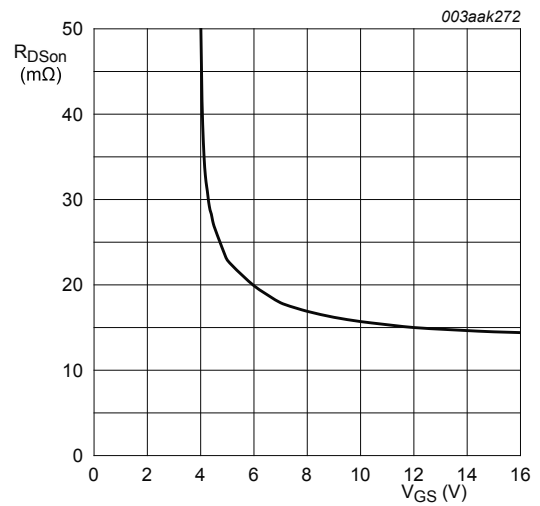


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25^\circ\text{C}; I_D = 10\text{ A}$

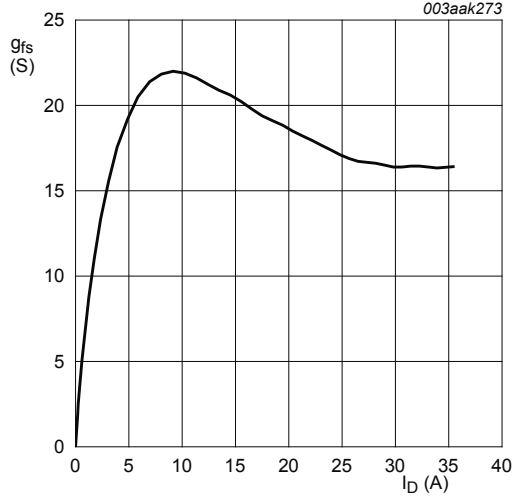


Fig. 8. Forward transconductance as a function of drain current; typical values

$$T_j = 25^\circ\text{C}; V_{DS} = 10\text{V}$$

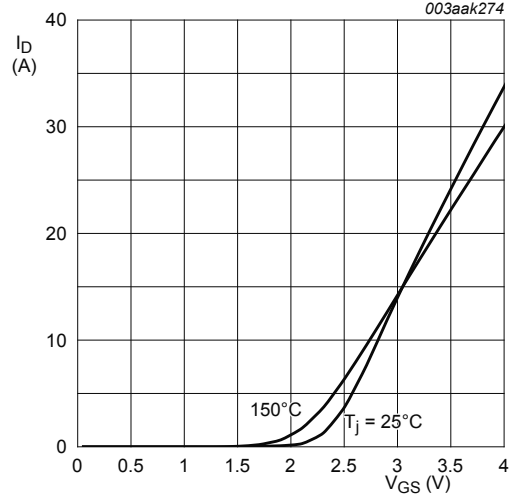


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$$V_{DS} = 10\text{V}$$

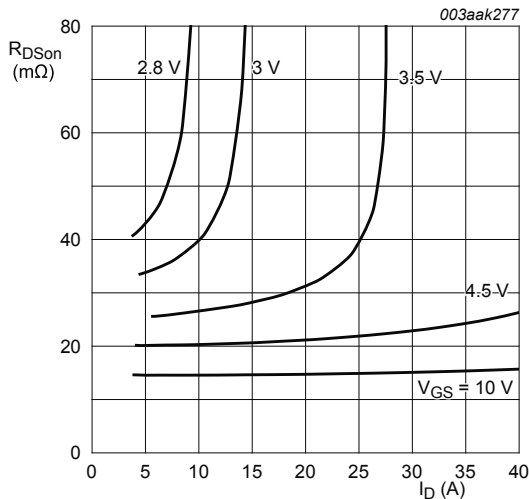


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

$$T_j = 25^\circ\text{C}$$

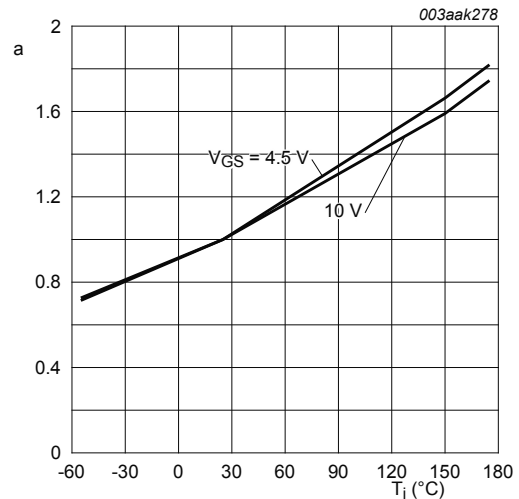


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

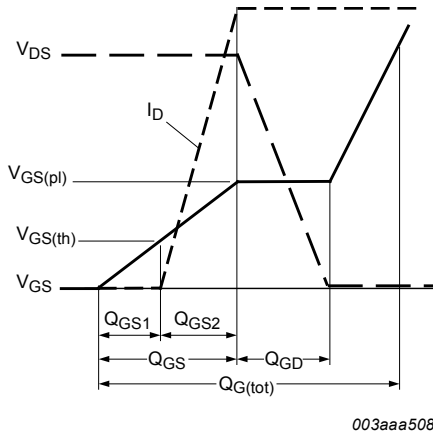


Fig. 12. Gate charge waveform definitions

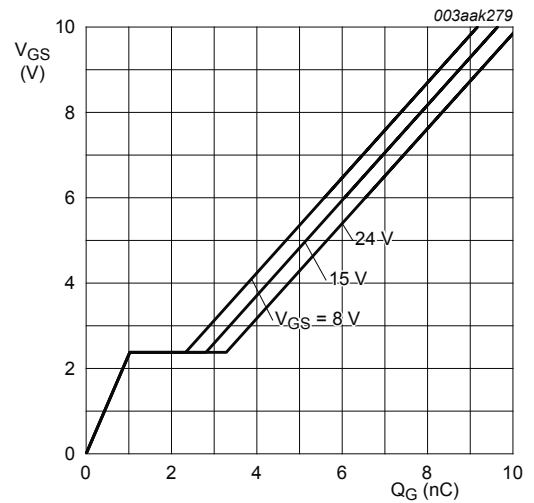


Fig. 13. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ\text{C}; I_D = 10\text{A}$

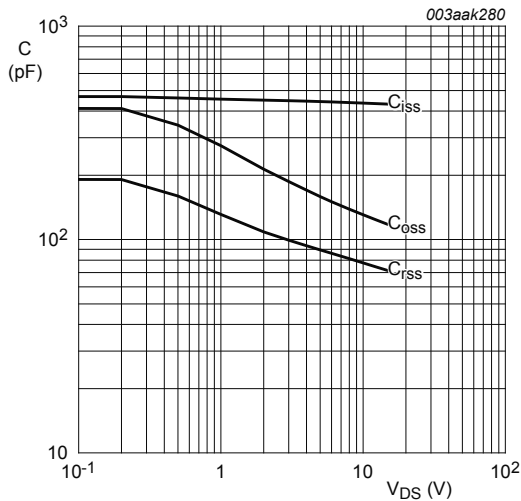


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{V}; f = 1\text{MHz}$

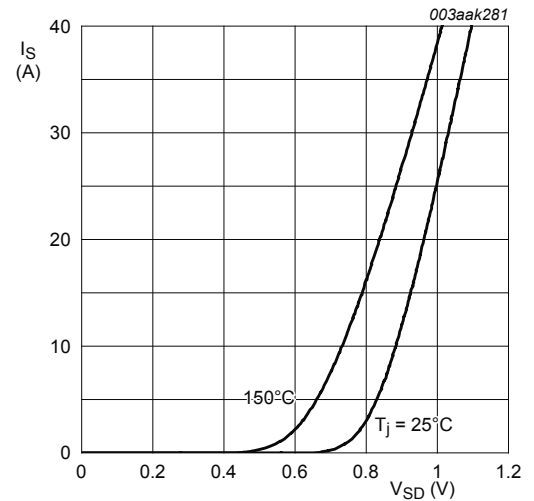


Fig. 15. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0\text{V}$

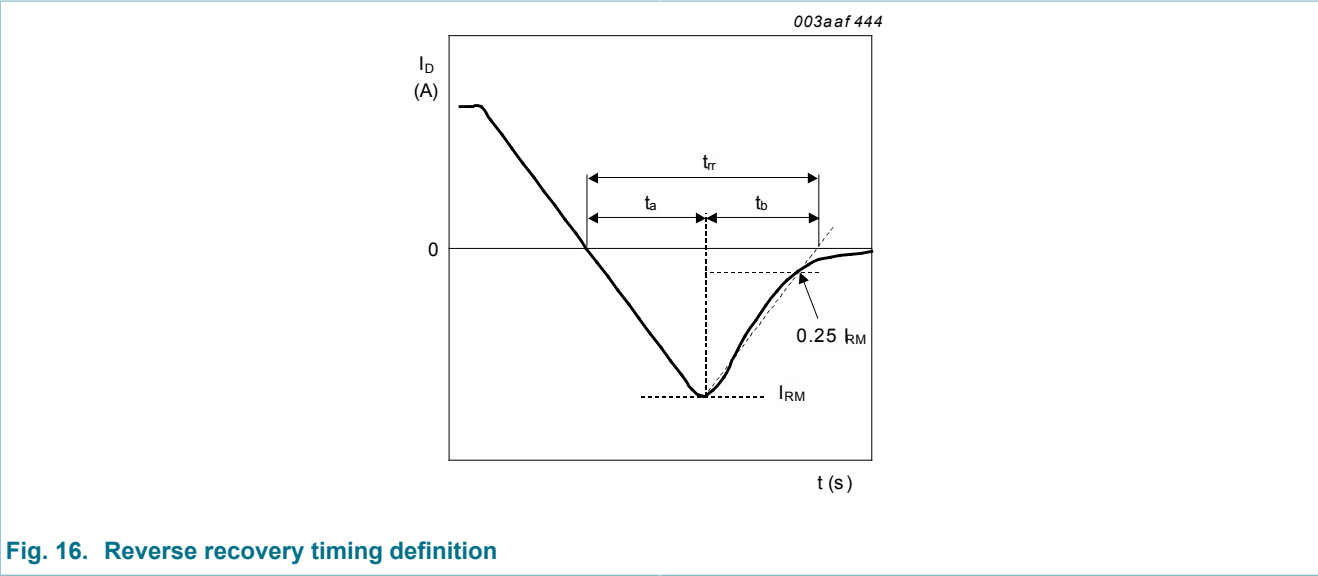


Fig. 16. Reverse recovery timing definition

7. Package outline

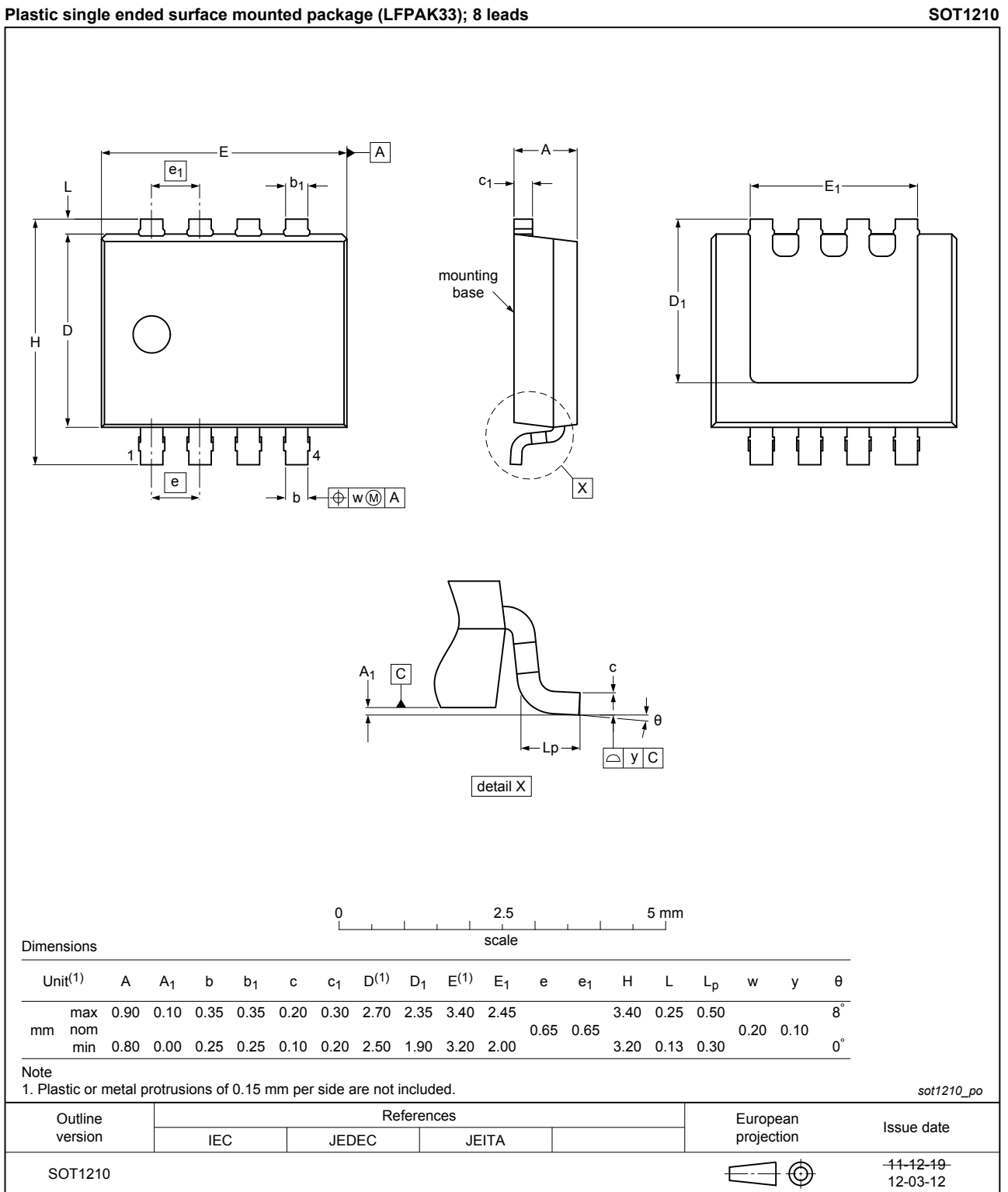


Fig. 17. Package outline LPAK33 (SOT1210)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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