BUK9Y19-55B

N-channel TrenchMOS logic level FET

Rev. 03 — 29 February 2008 | Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode power Field-Effect Transistor (FET) in a plastic package using NXP High-Performance Automotive (HPA) TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features

- 175 °C rated
- Q101 compliant
- Logic level compatible
- Very low on-state resistance

1.3 Applications

- 12 V and 24 V loads
- General purpose power switching
- Automotive systems
- Motors, lamps and solenoids

1.4 Quick reference data

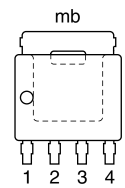
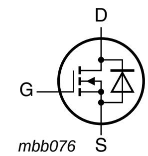
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_D	drain current	V_{GS} = 5 V; T_{mb} = 25 °C; see Figure 1 and 4	-	-	46	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2	-	-	85	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	V_{GS} = 5 V; I_D = 20 A; T_j = 25 °C; see Figure 12 and 13	-	16.3	19	mΩ
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 46 A; $V_{sup} \leq$ 55 V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped	-	-	80	mJ

founded by Philips

2. Pinning information

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 SOT669 (LFPAK)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9Y19-55B	LFPAK	plastic single-ended surface-mounted package (LFPAK); 4 leads	SOT669

4. Limiting values

Table 4. Limiting values

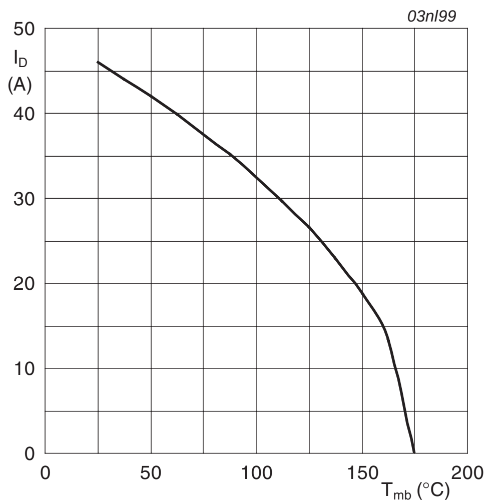
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	55	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20$ kΩ	-	55	V
V_{GS}	gate-source voltage		-15	15	V
I_D	drain current	$T_{mb} = 25$ °C; $V_{GS} = 5$ V; see Figure 1 and 4	-	46	A
		$T_{mb} = 100$ °C; $V_{GS} = 5$ V; see Figure 1	-	32	A
I_{DM}	peak drain current	$T_{mb} = 25$ °C; $t_p \leq 10$ µs; pulsed; see Figure 4	-	184	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2	-	85	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 46$ A; $V_{sup} \leq 55$ V; $R_{GS} = 50$ Ω; $V_{GS} = 5$ V; $T_{j(init)} = 25$ °C; unclamped	-	80	mJ
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	see Figure 3 [1][2][3]	-	-	J
Source-drain diode					
I_S	source current	$T_{mb} = 25$ °C	-	46	A
I_{SM}	peak source current	$t_p \leq 10$ µs; pulsed; $T_{mb} = 25$ °C	-	184	A

[1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

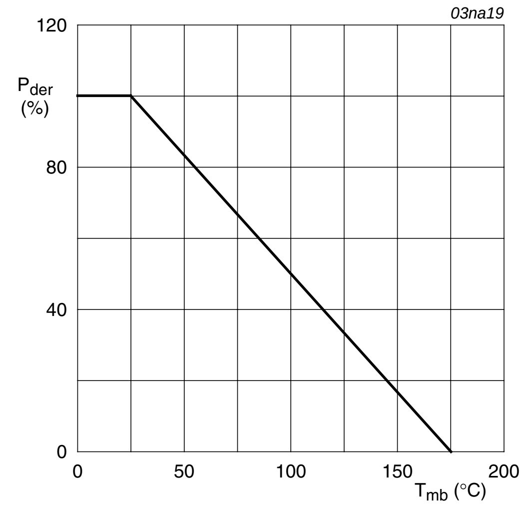
[2] Repetitive avalanche rating limited by average junction temperature of 170 °C.

[3] Refer to application note AN10273 for further information.



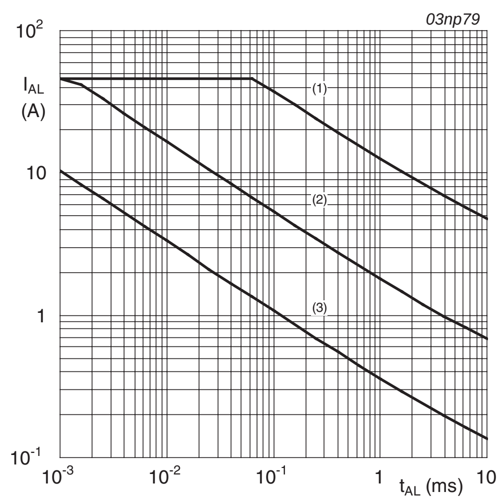
$V_{GS} \geq 5 V$

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature

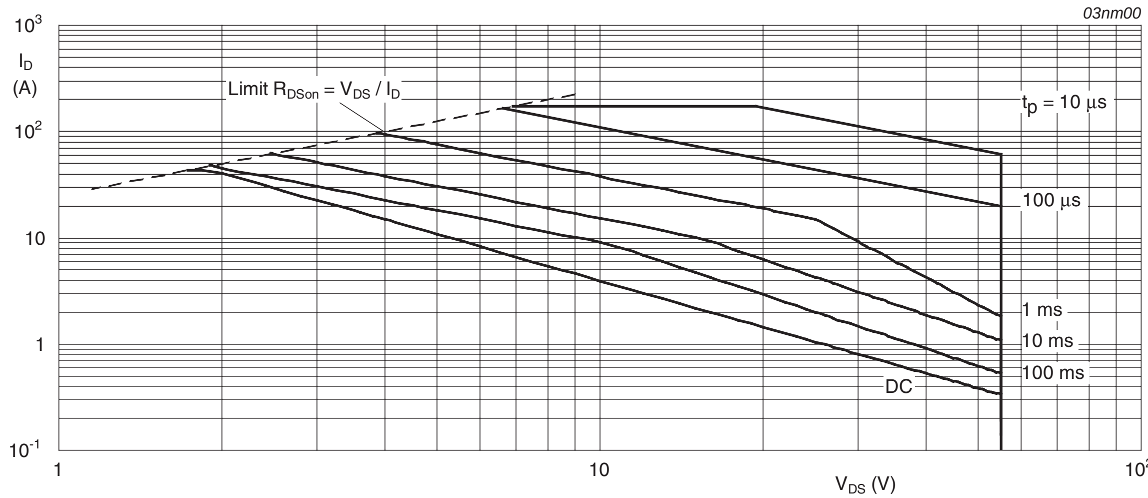


(1) Single−pulse; T_j = 25 °C.

(2) Single−pulse; T_j = 150 °C.

(3) Repetitive.

Fig 3. Single-shot and repetitive avalanche rating; avalanche current as a function of avalanche period



T_{mb} = 25 °C; I_{DM} is single pulse

Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	-	1.8	K/W

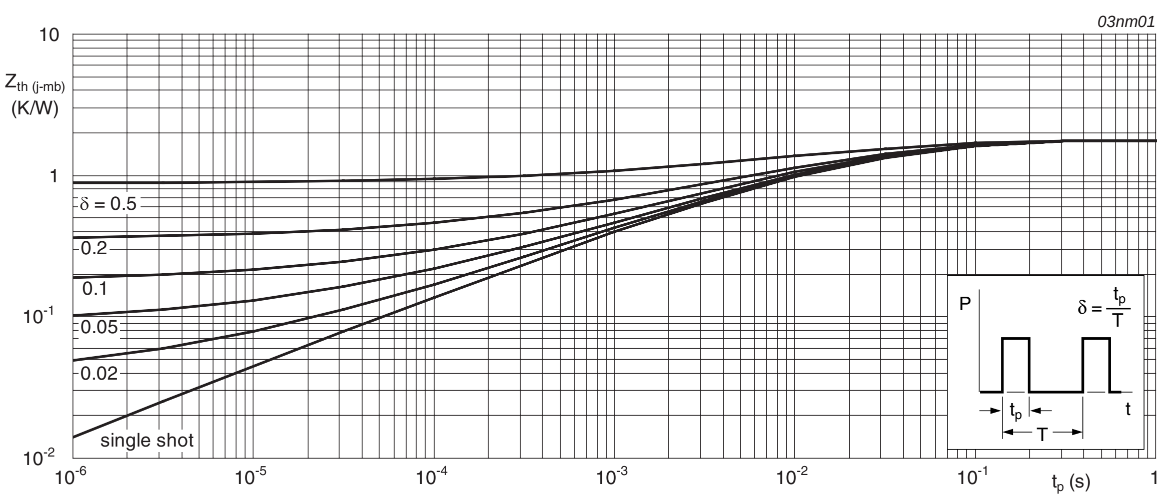
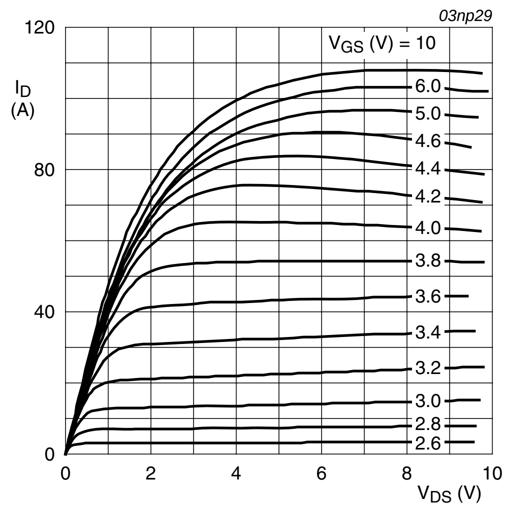


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

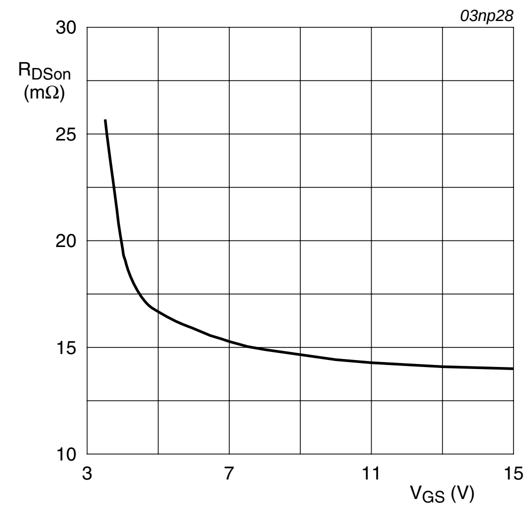
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V; T_j = 25 °C	55	-	-	V
		I_D = 0.25 mA; V_{GS} = 0 V; T_j = -55 °C	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 11	-	-	2.3	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 11	1.1	1.5	2	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; see Figure 11	0.5	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 55 V; V_{GS} = 0 V; T_j = 175 °C	-	-	500	µA
		V_{DS} = 55 V; V_{GS} = 0 V; T_j = 25 °C	-	0.02	1	µA
I_{GSS}	gate leakage current	V_{DS} = 0 V; V_{GS} = 15 V; T_j = 25 °C	-	2	100	nA
		V_{DS} = 0 V; V_{GS} = -15 V; T_j = 25 °C	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 20 A; T_j = 25 °C	-	-	21	mΩ
		V_{GS} = 10 V; I_D = 20 A; T_j = 25 °C	-	14.3	17.3	mΩ
		V_{GS} = 5 V; I_D = 20 A; T_j = 25 °C; see Figure 12 and 13	-	16.3	19	mΩ
		V_{GS} = 5 V; I_D = 20 A; T_j = 175 °C; see Figure 12 and 13	-	-	40	mΩ
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 16	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = -10 V; V_{DS} = 30 V; T_j = 25 °C	-	52	-	ns
Q_r	recovered charge		-	38	-	nC
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 44 V; V_{GS} = 5 V; T_j = 25 °C; see Figure 14	-	18	-	nC
Q_{GS}	gate-source charge		-	5	-	nC
Q_{GD}	gate-drain charge		-	8	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; see Figure 15	-	1494	1992	pF
C_{oss}	output capacitance		-	217	260	pF
C_{rss}	reverse transfer capacitance		-	86	118	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 10 Ω; T_j = 25 °C	-	18	-	ns
t_r	rise time		-	180	-	ns
$t_{d(off)}$	turn-off delay time		-	44	-	ns
t_f	fall time		-	134	-	ns



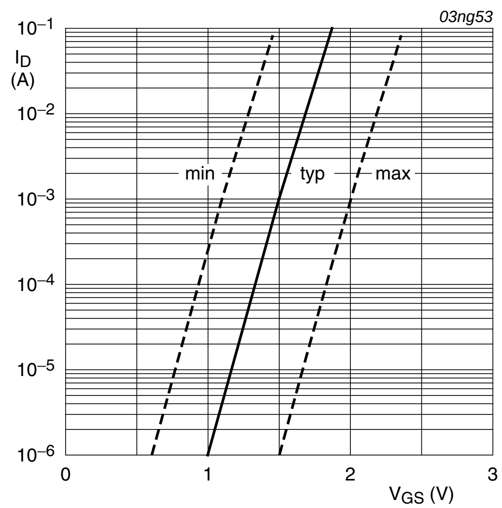
$T_j = 25\,°C; t_p = 300\,\mu s$

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



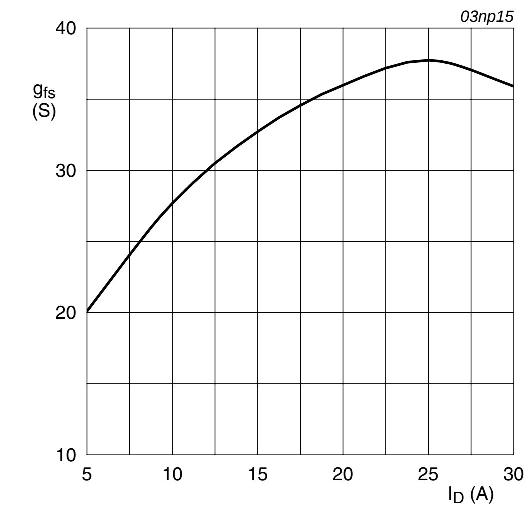
$T_j = 25\,°C; I_D = 20\,A$

Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



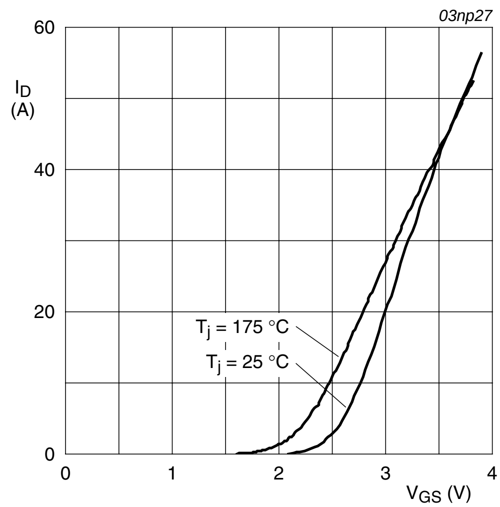
$T_j = 25\,°C; V_{DS} = V_{GS}$

Fig 8. Sub-threshold drain current as a function of gate-source voltage



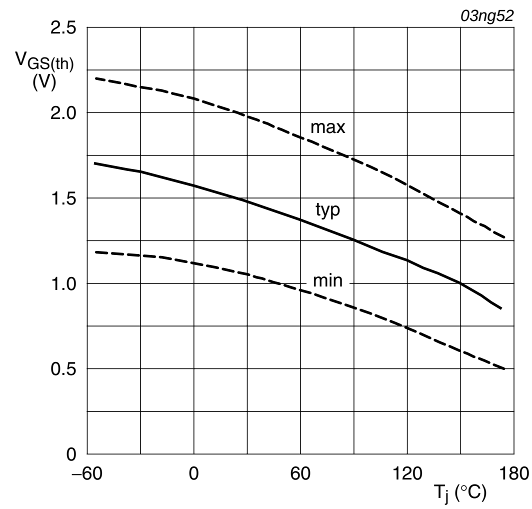
$T_j = 25\,°C; V_{DS} = 25\,V$

Fig 9. Forward transconductance as a function of drain current; typical values



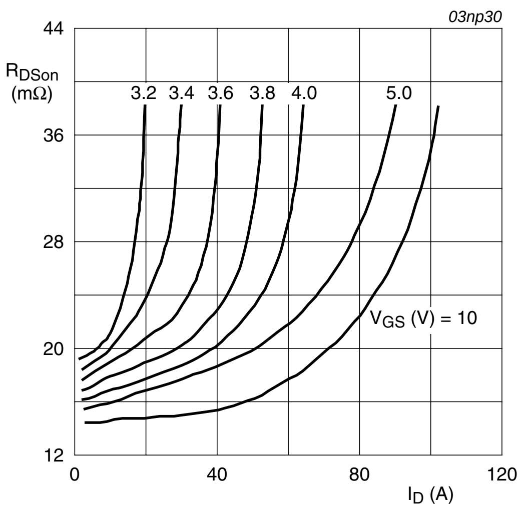
$V_{DS} = 25 V$

Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



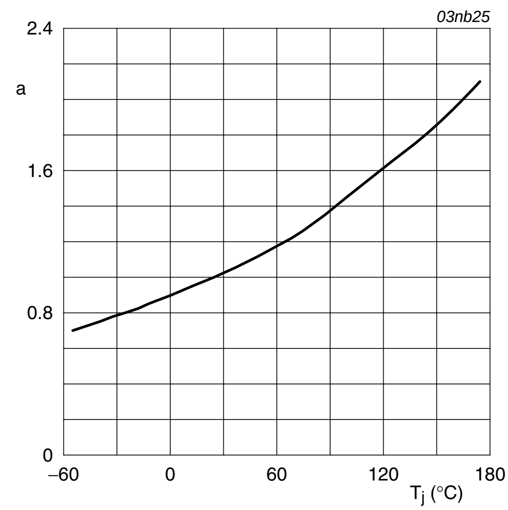
$I_D = 1 mA; V_{DS} = V_{GS}$

Fig 11. Gate-source threshold voltage as a function of junction temperature



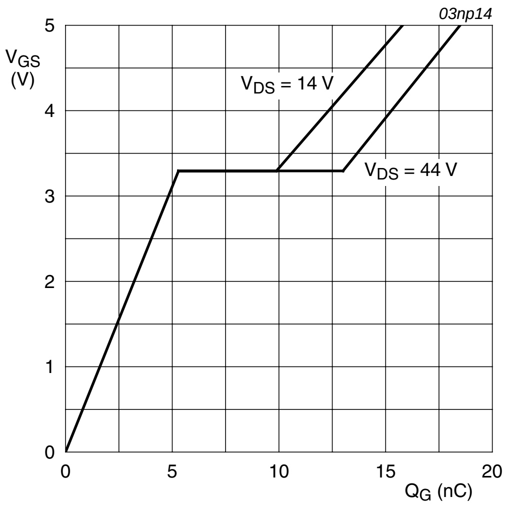
$T_j = 25 °C$

Fig 12. Drain-source on-state resistance as a function of drain current; typical values



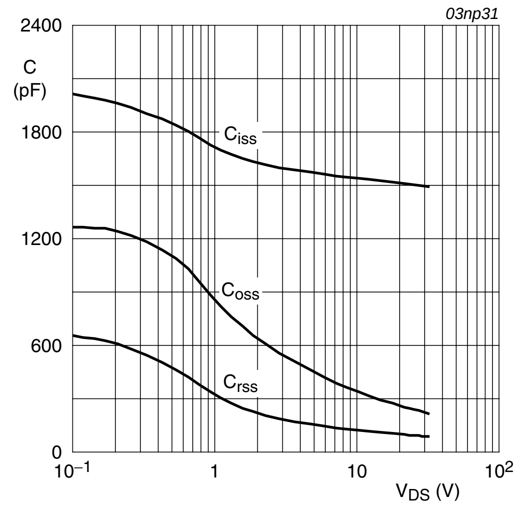
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature



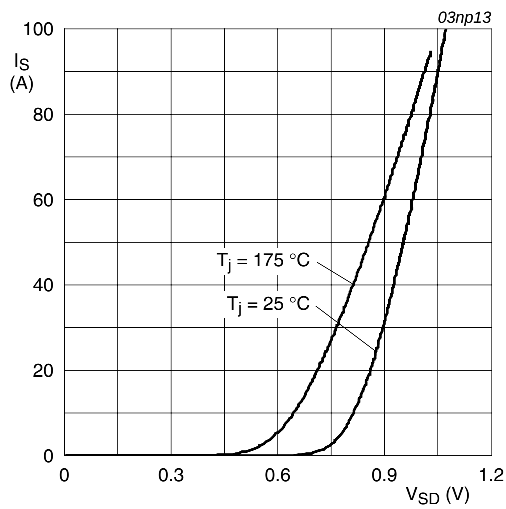
$T_j = 25\,°C; I_D = 25\,A$

Fig 14. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\,V;\ f = 1\,MHz$

Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

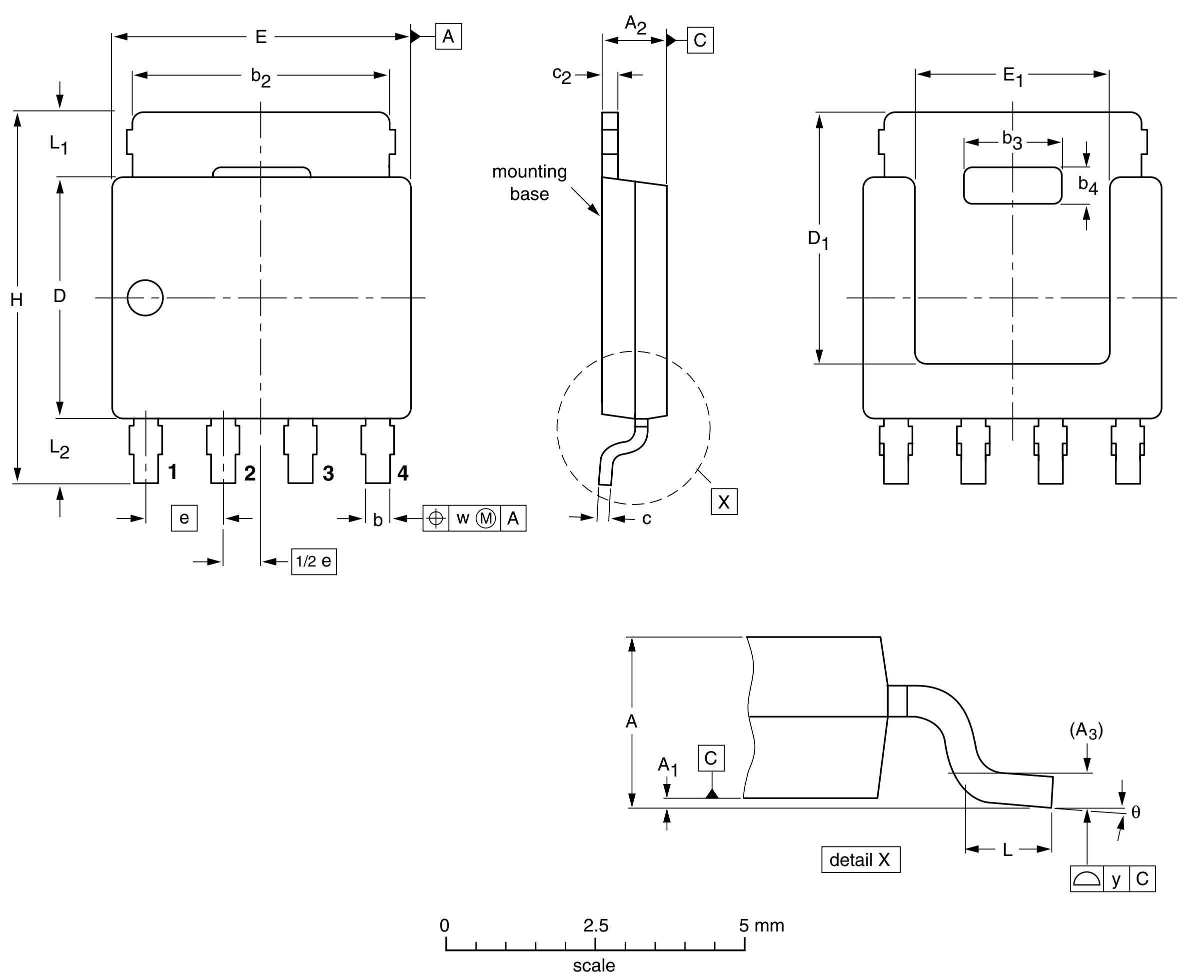


$V_{GS} = 0\,V$

Fig 16. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LFPAK); 4 leads **SOT669**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	A_2	A_3	b	b_2	b_3	b_4	c	c_2	D(1)	D_1(1) max	E(1)	E_1(1)	e	H	L	L_1	L_2	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT669		MO-235				~~04-10-13~~ 06-03-16

Fig 17. Package outline SOT669 (LFPAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9Y19-55B_3	20080229	Product data sheet	-	BUK9Y19-55B_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
BUK9Y19-55B_2	20060411	Product data sheet	-	BUK9Y19-55B-01
BUK9Y19-55B-01 (9397 750 13188)	20040528	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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