

# BUK9C10-65BIT

## N-channel TrenchPLUS logic level FET

Rev. 02 — 21 June 2010

Product data sheet

## 1. Product profile

### 1.1 General description

N-channel enhancement mode field-effect power transistor in SOT427. Device is manufactured using NXP High-Performance TrenchPLUS technology, featuring very low on-state resistance, integrated current sensing transistors and over temperature protection diodes.

### 1.2 Features and benefits

- AEC-Q101 compliant
- Low conduction losses due to low on-state resistance

### 1.3 Applications

- Lamp switching
- Motor drive systems
- Power distribution
- Solenoid drivers

### 1.4 Quick reference data

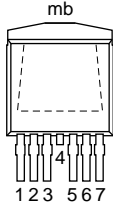
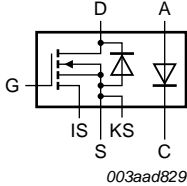
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 13</a> ; see <a href="#">Figure 12</a>	-	8.5	10	mΩ
$I_D/I_{sense}$	ratio of drain current to sense current	$T_j = 25\text{ °C}$ ; $V_{GS} = 5\text{ V}$ ; see <a href="#">Figure 14</a>	8094	8993	9892	A/A
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ μA}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$	65	-	-	V



## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p><b>SOT427 (D2PAK)</b></p>	 <p>003aad829</p>
2	IS	current sense		
3	A	anode		
4	D	drain		
5	K	cathode		
6	KS	Kelvin source		
7	S	source		
mb	D	mb		

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		Version
	Name	Description	
BUK9C10-65BIT	D2PAK	plastic single-ended surface-mounted package (D2PAK); 7 leads (one lead cropped)	SOT427

## 4. Limiting values

**Table 4. Limiting values**

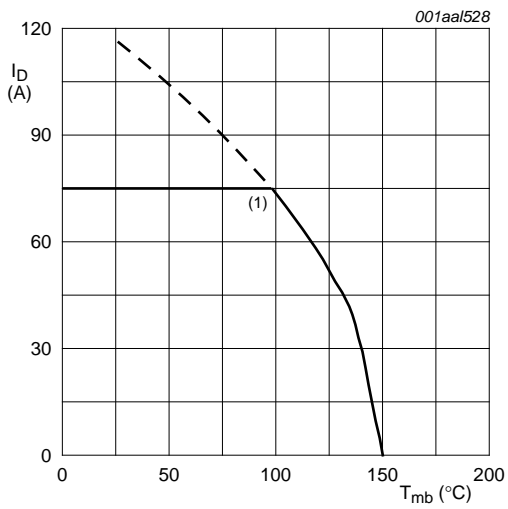
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-	65	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$ ; $25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	-	65	V
$V_{GS}$	gate-source voltage		-15	-	15	V
$I_D$	drain current	$V_{GS} = 5\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a> <sup>[1]</sup>	-	-	75	A
		$V_{GS} = 5\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 1</a> <sup>[1]</sup>	-	-	60	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; single pulse; $t_p \leq 10\text{ }\mu\text{s}$ ; see <a href="#">Figure 4</a>	-	-	346	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	171	W
$T_{stg}$	storage temperature		-55	-	150	°C
$T_j$	junction temperature		-55	-	150	°C
$V_{isol(FET-TSD)}$	FET to temperature sense diode isolation voltage		-	-	100	V
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25\text{ °C}$ <sup>[1]</sup>	-	-	75	A
$I_{SM}$	peak source current	single pulse; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	-	346	A
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}$ ; $V_{sup} = 65\text{ V}$ ; $V_{GS} = 5\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped; see <a href="#">Figure 3</a> <sup>[2][3]</sup>	-	-	0.214	J
<b>Electrostatic discharge</b>						
$V_{ESD}$	electrostatic discharge voltage	HBM; $C = 100\text{ pF}$ ; $R = 1.5\text{ k}\Omega$ ; all pins	-	-	0.15	kV
		HBM; $C = 100\text{ pF}$ ; $R = 1.5\text{ k}\Omega$ ; pin 4 to pin 7	-	-	4	kV

[1] Current is limited by package

[2] Single-pulse avalanche rating limited by maximum junction temperature of 150 °C.

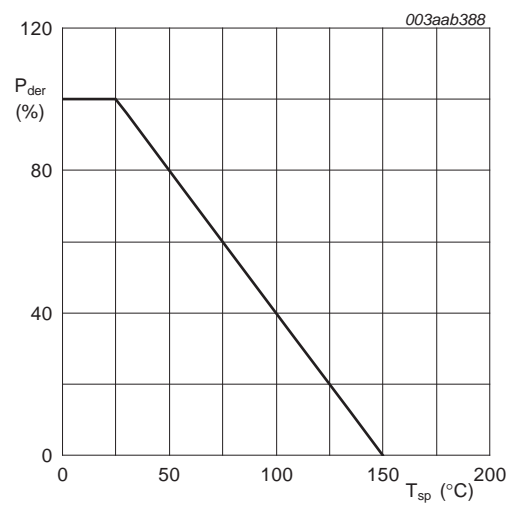
[3] Refer to application note AN10273 for further information.



$$V_{GS} \geq 5V$$

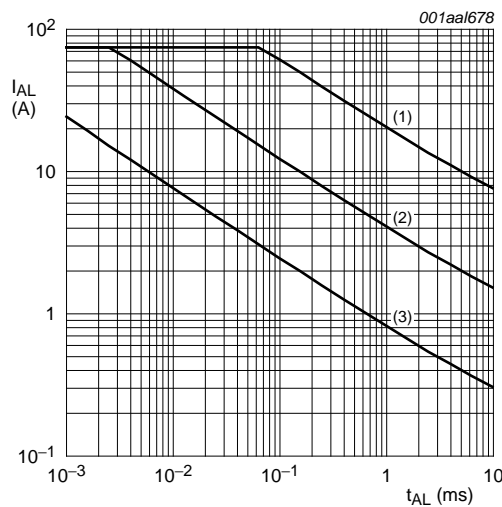
(1) Current is limited by package

**Fig 1. Continuous drain current as a function of solder point temperature**



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

**Fig 2. Normalized total power dissipation as a function of solder point temperature**



- (1) Single-pulse;  $T_j = 25^{\circ}C$ .
- (2) Single-pulse;  $T_j = 150^{\circ}C$ .
- (3) Repetitive.

**Fig 3. Single-Pulse and repetitive avalanche rating; avalanche current as a function of avalanche time.**

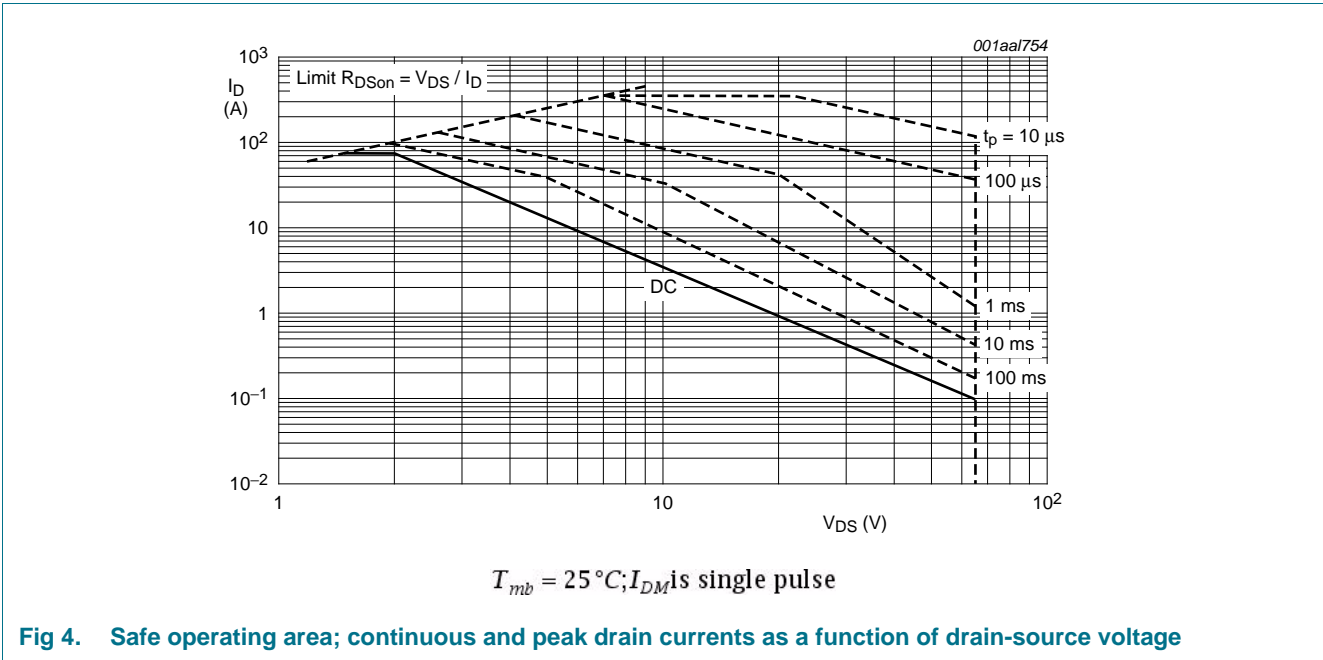


Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 5</a>	-	-	0.73	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	61	-	K/W

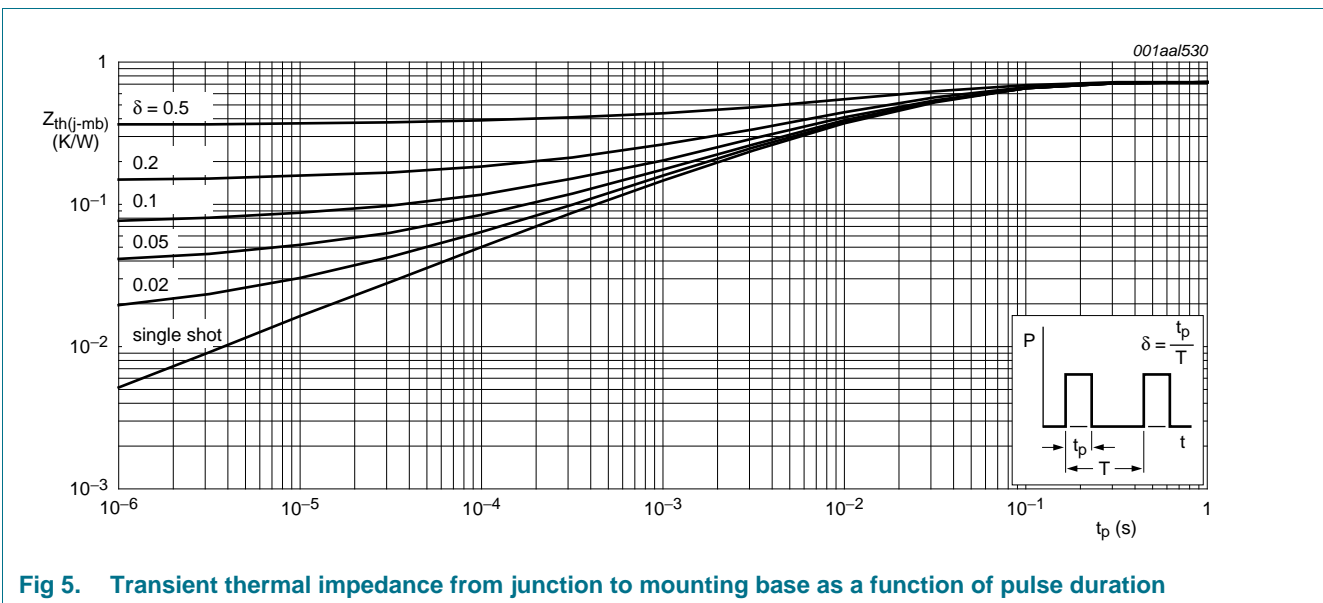


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

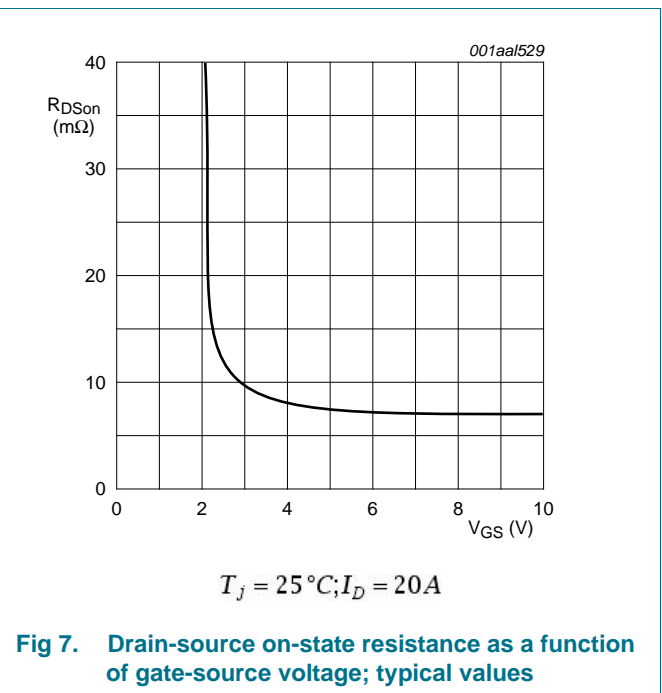
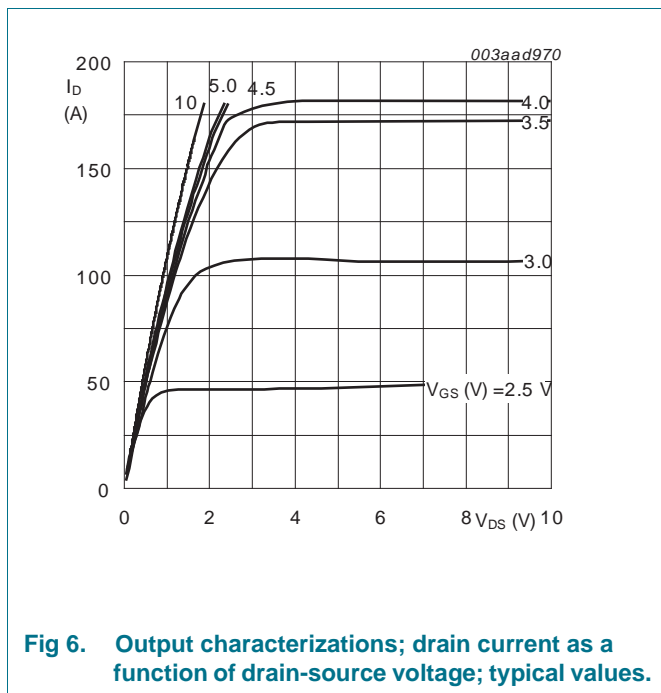
## 6. Characteristics

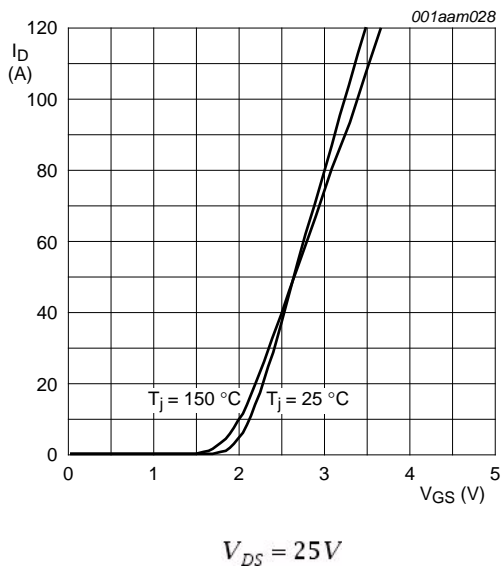
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	65	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	59	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	1	1.5	2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	-	-	2.3	V
$I_{DSS}$	drain leakage current	$V_{DS} = 52 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	3	$\mu\text{A}$
		$V_{DS} = 52 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	125	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = 15 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	300	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	-	11	m $\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 13</a> ; see <a href="#">Figure 12</a>	-	8.5	10	m $\Omega$
		$V_{GS} = 5 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 13</a> ; see <a href="#">Figure 12</a>	-	-	20	m $\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 13</a> ; see <a href="#">Figure 12</a>	-	-	8.3	m $\Omega$
$I_D/I_{sense}$	ratio of drain current to sense current	$V_{GS} = 5 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 14</a>	8094	8993	9892	A/A
$S_{F(TSD)}$	temperature sense diode temperature coefficient	$I_F = 250 \mu\text{A}; 25 \text{ }^\circ\text{C} \leq T_j \leq 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 15</a>	-5.4	-5.7	-6	mV/K
$V_{F(TSD)}$	temperature sense diode forward voltage	$I_F = 250 \mu\text{A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 15</a>	2.855	2.9	2.945	V
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 20 \text{ A}; V_{DS} = 52 \text{ V}; V_{GS} = 5 \text{ V};$ see <a href="#">Figure 16</a>	-	59.6	-	nC
$Q_{GS}$	gate-source charge		-	10.4	-	nC
$Q_{GD}$	gate-drain charge		-	21.6	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 17</a>	-	4170	-	pF
$C_{oss}$	output capacitance		-	521	-	pF
$C_{rSS}$	reverse transfer capacitance		-	194	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.5 \text{ } \Omega; V_{GS} = 5 \text{ V};$ $R_{G(ext)} = 10 \text{ } \Omega$	-	40	-	ns
$t_r$	rise time		-	113	-	ns
$t_{d(off)}$	turn-off delay time		-	193	-	ns
$t_f$	fall time		-	108	-	ns
$L_D$	internal drain inductance	from pin to center of die	-	0.9	-	nH

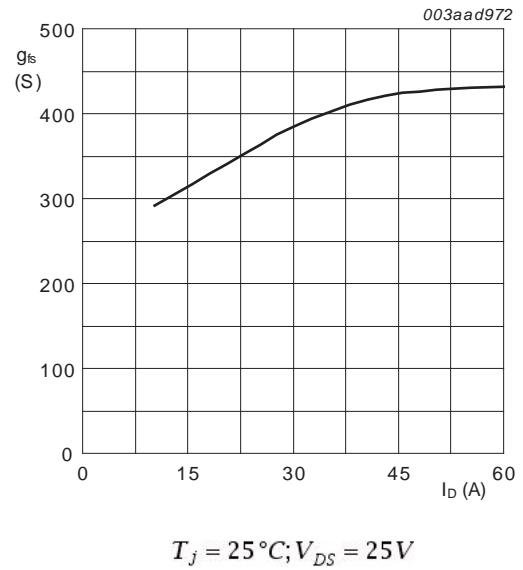
**Table 6. Characteristics ...continued**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$L_S$	internal source inductance	from source lead to source bonding pad	-	2	-	nH
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 10\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 18</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 10\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ;	-	51	-	ns
$Q_r$	recovered charge	$V_{GS} = -10\text{ V}$ ; $V_{DS} = 30\text{ V}$	-	0.12	-	nC

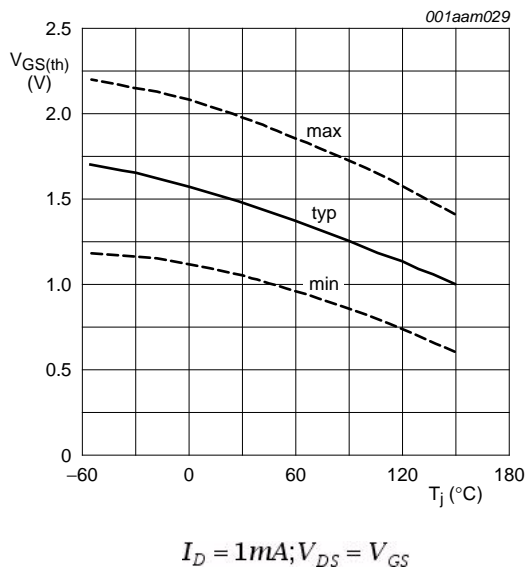




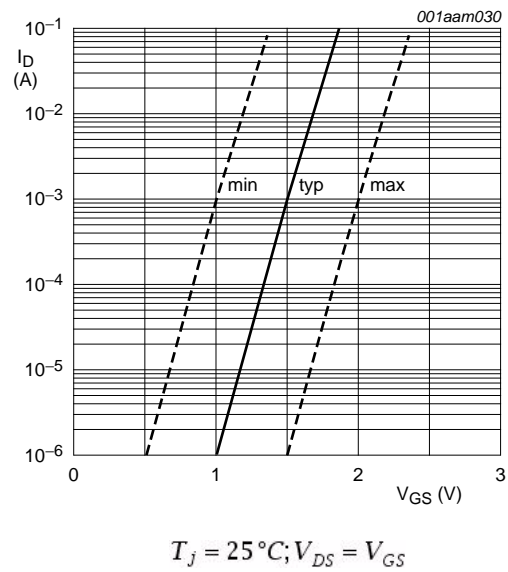
**Fig 8. Transfer Characteristics; drain current as a function of gate-source voltage; typical values.**



**Fig 9. Forward transconductance as a function of drain current; typical values.**

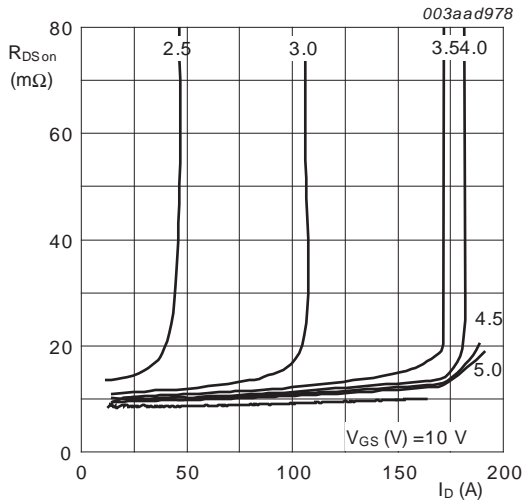


**Fig 10. Gate-source threshold voltage as a function of junction temperature.**

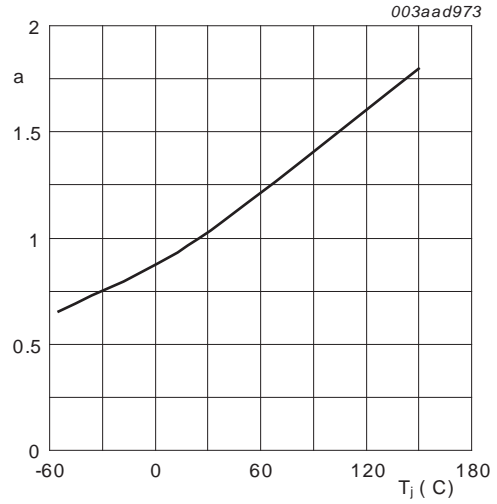


**Fig 11. Sub-threshold drain current as a function of gate-source voltage.**



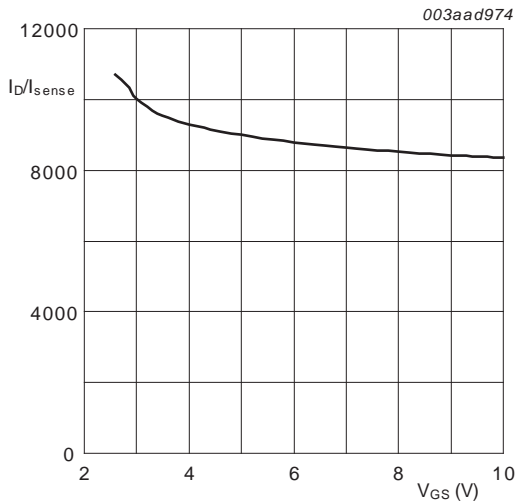


**Fig 12. Drain-source on-state resistance as a function of drain current; typical values**



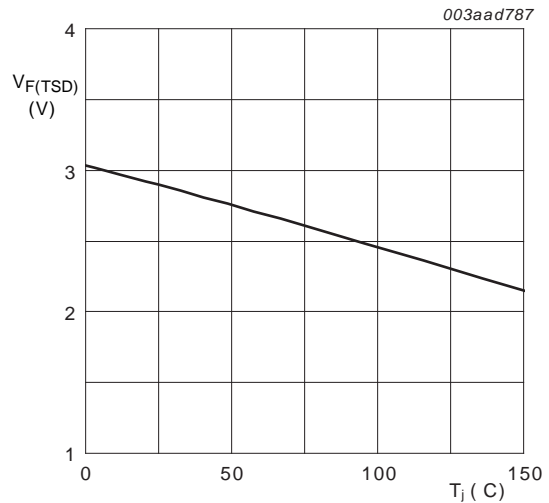
$$a = \frac{R_{DS(on)}}{R_{DS(on)@25^{\circ}C}}$$

**Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature**



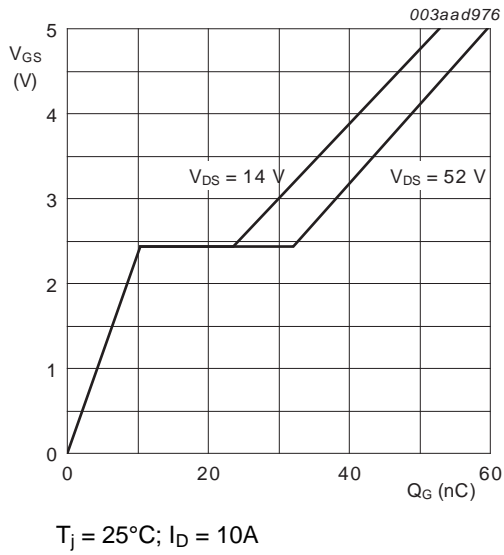
$$T_j = 25^{\circ}C; I_D = 25A$$

**Fig 14. Ratio of drain current to sense current as a function of gate-source voltage; typical values**

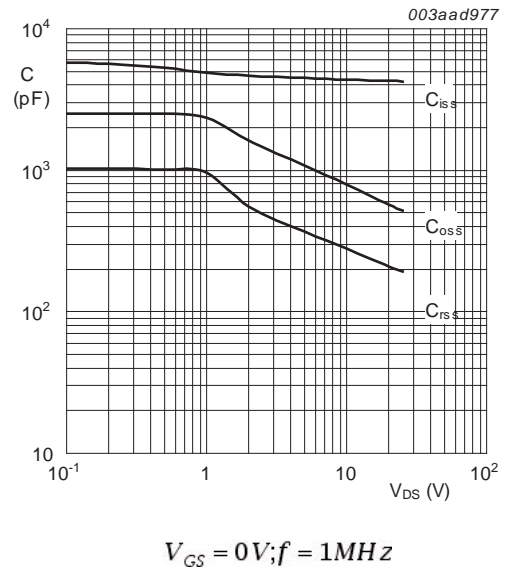


$$I_F = 250\mu A$$

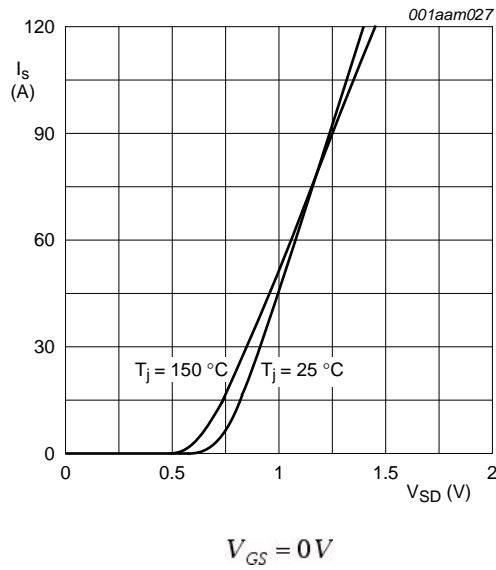
**Fig 15. Temperature sense diode forward voltage as a function of junction temperature**



**Fig 16. Gate-source voltage as a function of turn-on gate charge; typical values**



**Fig 17. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



**Fig 18. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values**

**7. Package outline**

Plastic single-ended surface-mounted package (D2PAK); 7 leads (one lead cropped)

SOT427

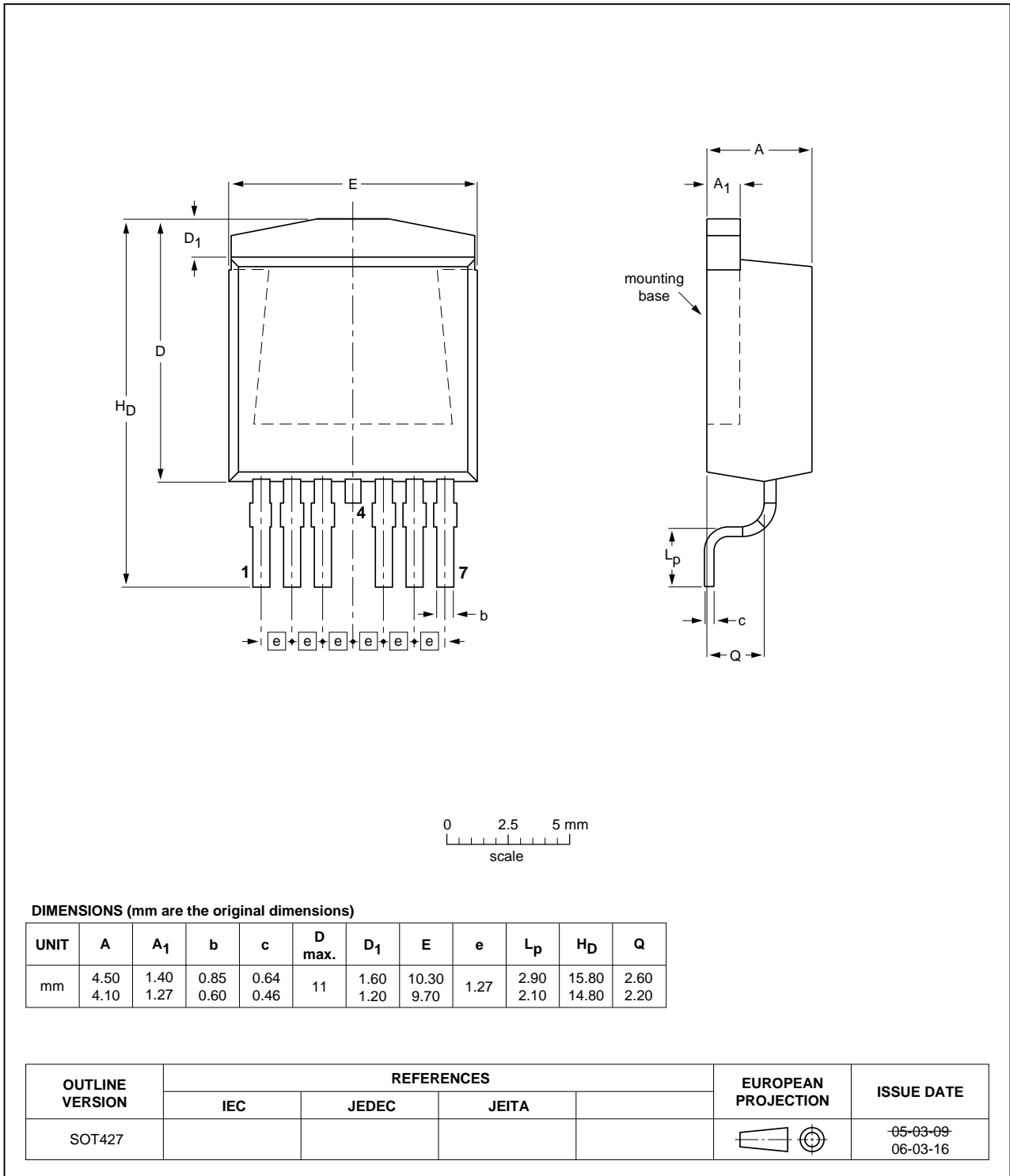


Fig 19. Package outline SOT427 (D2PAK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9C10-65BIT v.2	20100621	Product data sheet	-	BUK9C10-65BIT v.1
Modifications:	• Status changed from preliminary to product.			
BUK9C10-65BIT v.1	20100531	Preliminary data sheet	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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**11. Contents**

**1 Product profile . . . . .1**

1.1 General description . . . . .1

1.2 Features and benefits . . . . .1

1.3 Applications . . . . .1

1.4 Quick reference data . . . . .1

**2 Pinning information . . . . .2**

**3 Ordering information . . . . .2**

**4 Limiting values . . . . .3**

**5 Thermal characteristics . . . . .5**

**6 Characteristics . . . . .6**

**7 Package outline . . . . .11**

**8 Revision history . . . . .12**

**9 Legal information . . . . .13**

9.1 Data sheet status . . . . .13

9.2 Definitions . . . . .13

9.3 Disclaimers . . . . .13

9.4 Trademarks . . . . .14

**10 Contact information . . . . .14**

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 Document identifier: BUK9C10-65BIT